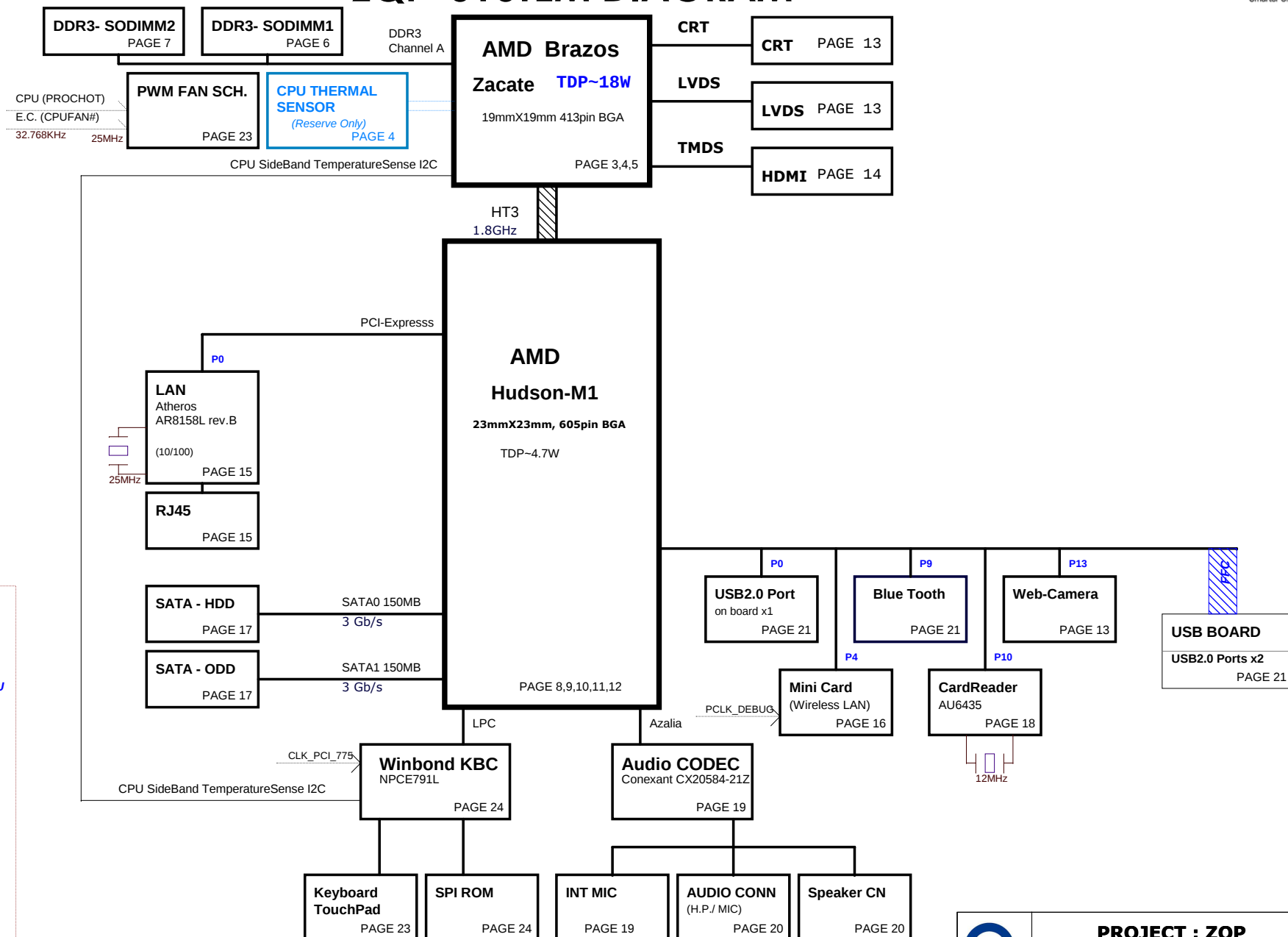
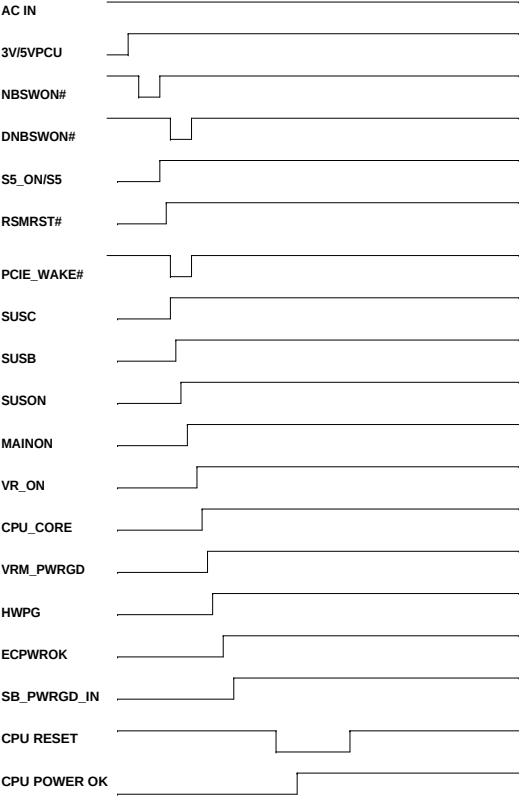


ZQP SYSTEM DIAGRAM



PAGE#	DESCRIPTION	NOTE
1	BLOCK DIAGRAM	
2	SYSTEM INFORMATION	
3	ONTARIO MEM & PCIE I/F(1/3)	
4	ONTATIO DISPLAY/CLK/MI(2/3)	
5	ONTARIO POWER & DECOUP(3/3)	
6	DDR3 SO-DIMM (STD=8)	
7	DDR3 SO-DIMM (STD=4)	
8	HUDSON PCIE/LPC/CPU IF(1/5)	
9	HUDSON ACPI/GPIO/USB(2/5)	
10	HUDSON SATA/BIDs(3/5)	
11	HUDSON PWR/GND(4/5)	
12	HUDSON STRAPS/PWRGD(5/5)	
13	CRT/LVDS/CCD	
14	HDMI	
15	LAN AR8152	
16	MINI PCI-E	
17	HDD /ODD	
18	CARD READER	
19	AUDIO - CONEXANT 20584	
20	AUDIO JACK CONN	
21	USB / BT /TP	
22	LED / NUT	
23	KB/FAN/TP	
24	WPCE791 /FLASH	
25	CHARGER (ISL88731A)	
26	SYSTEM 5V/3V (RT8223M)	
27	CPU CORE (OZ8380)	
28	VCCP 1.1V (G5602)	
29	+1V(G5602)	
30	DDR 1.5V (RT8207A)	
31	+1.8V/Discharge/Thermal Protection	
32	Change list	

Power Sequence



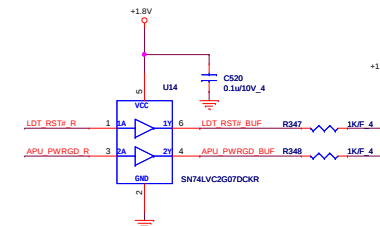
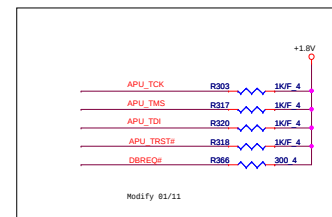
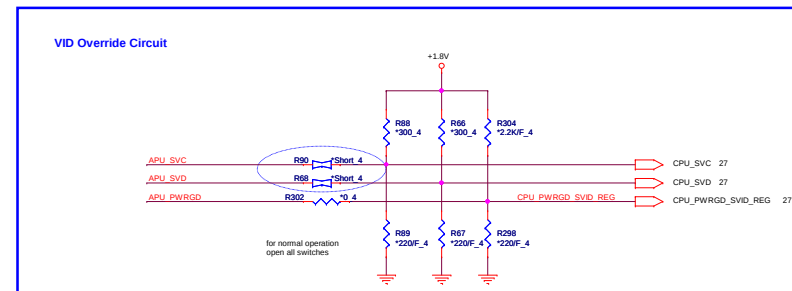
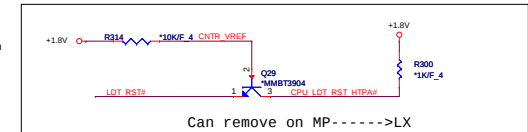
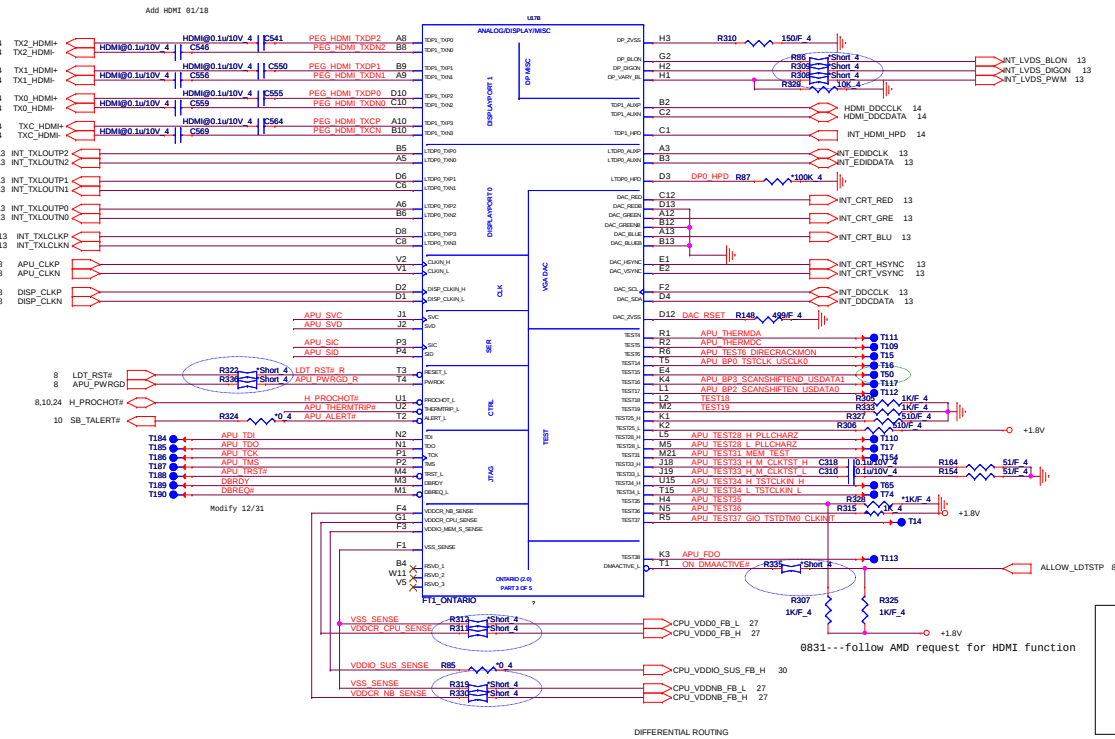
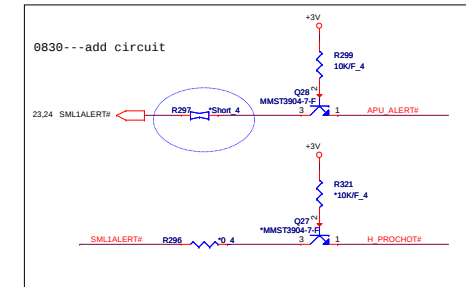
Hudson M1 SM BUS

SB820 SMBUS	Pin NO.	SMBUS Function Define
PCLK_SMB PDAT_SMB (+3V)	AD22 AE22	DDR / RFID
SB_SMBCLK1 SB_SMBDATA1 (+3V_S5)	F5 F4	not used
SB_SCLK2 SB_SDATA2 (+3V_S5)	D25 F23	not used
SB_SCLK3 SB_SDATA3 (+3V_S5)	B26 E26	not used
SB_SCLK3 SB_SDATA3 (+3V_S5)	B26 E26	not used

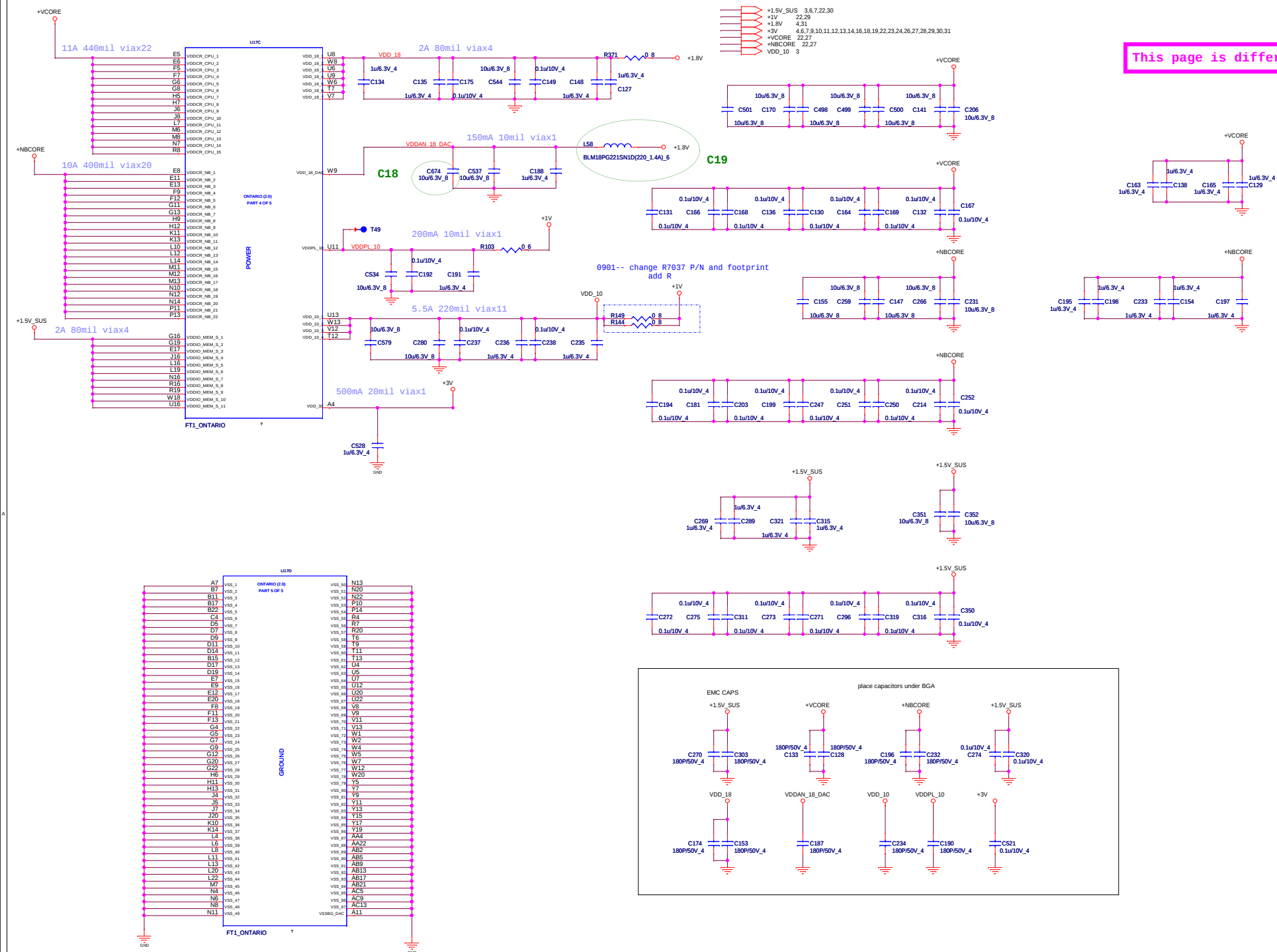
KBC(EC) SM BUS

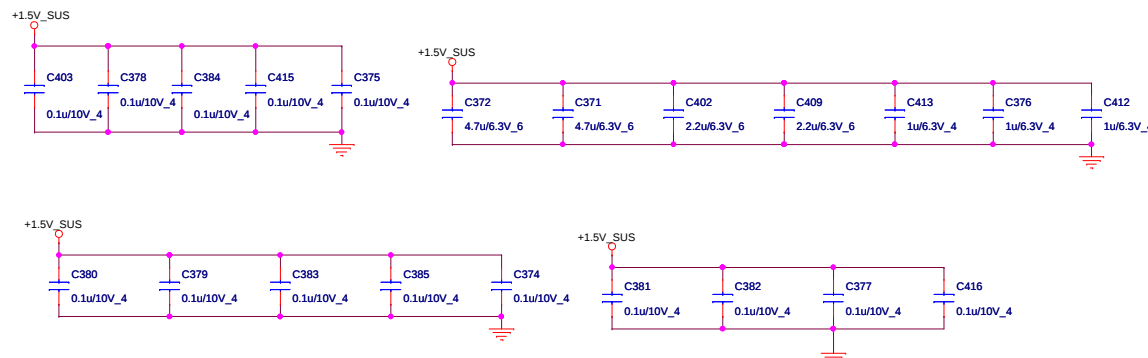
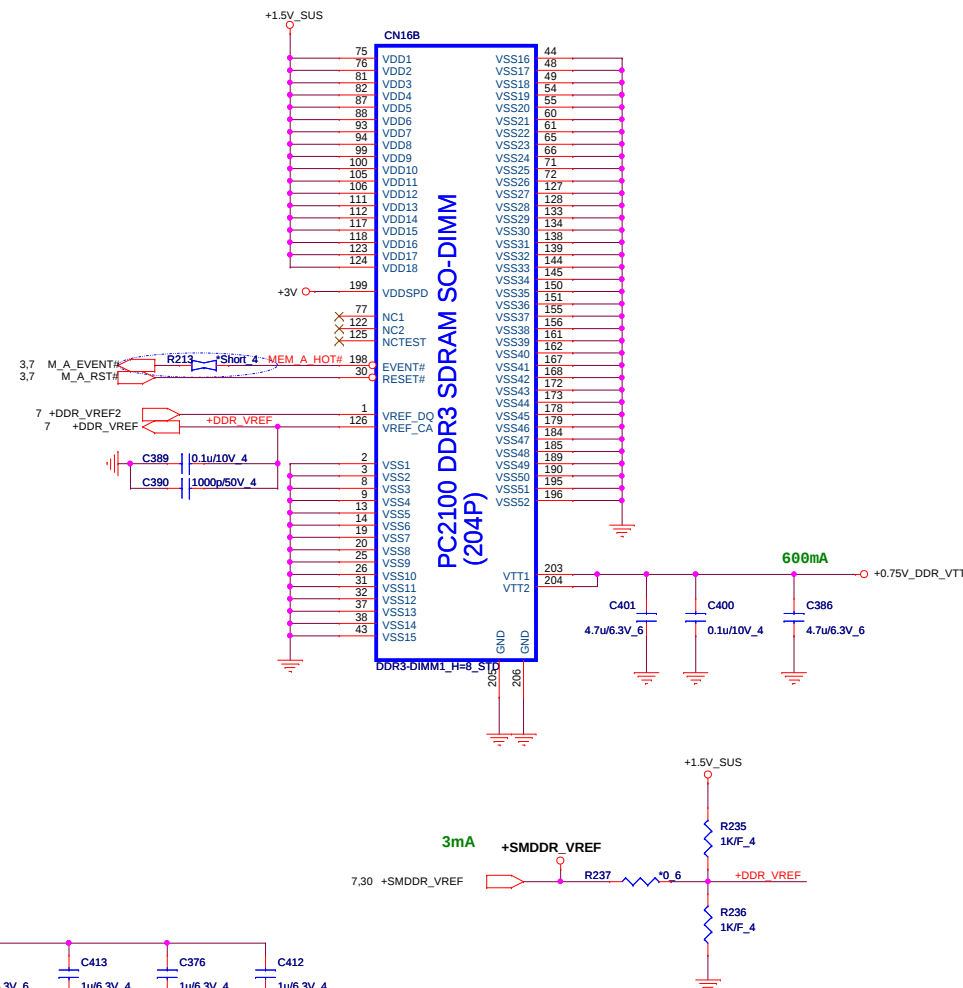
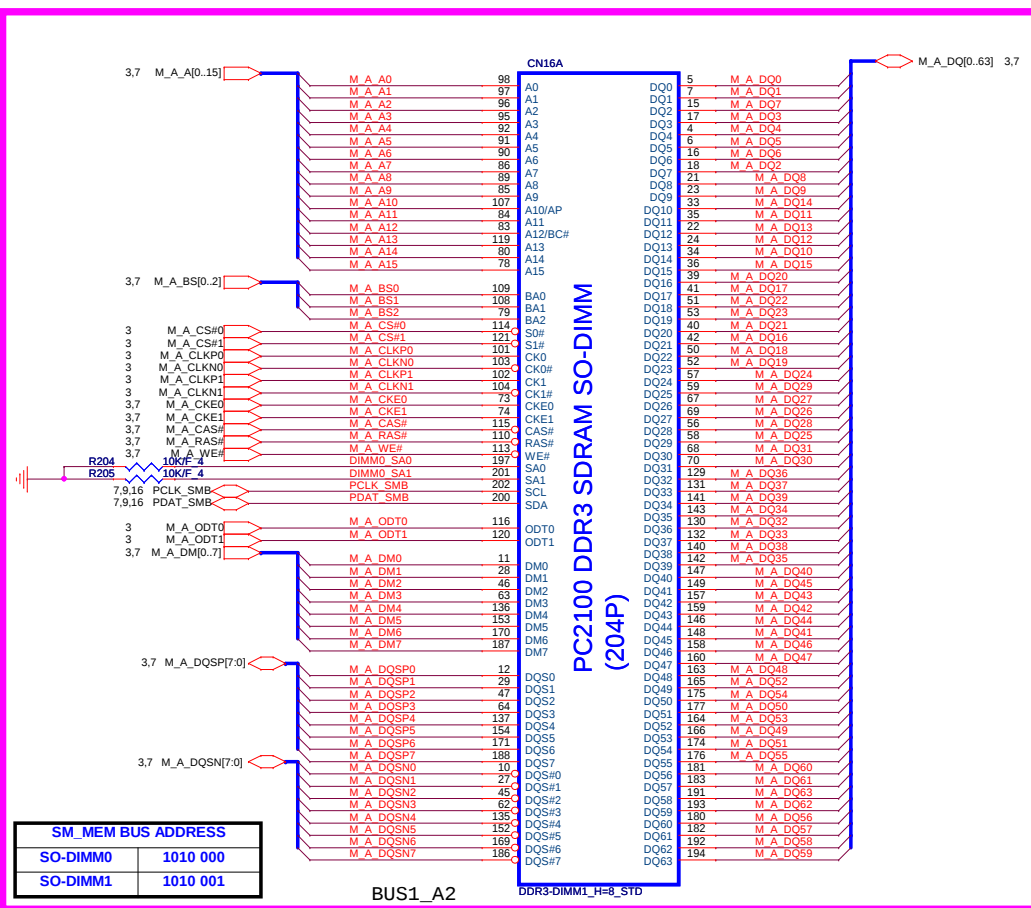
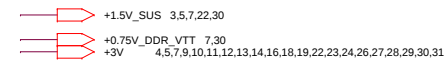
KBC SMBUS	Pin NO.	SMBUS Function Define
MBCLK MBDATA (+3VPCU)	110 111	Battery
MBCLK_THRM MBDATA_THRM (+3VPCU)	115 116	Thermal





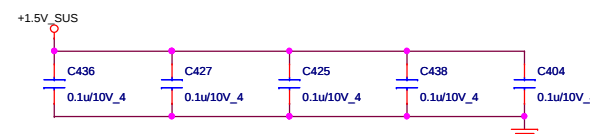
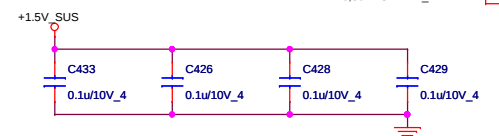
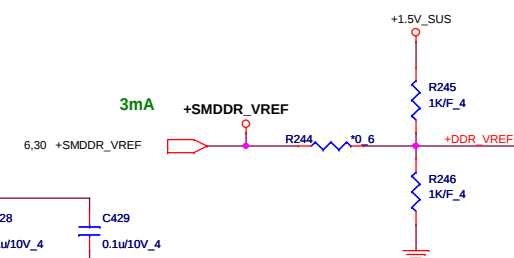
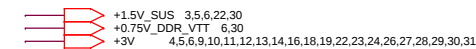
This page is different AMD Nil





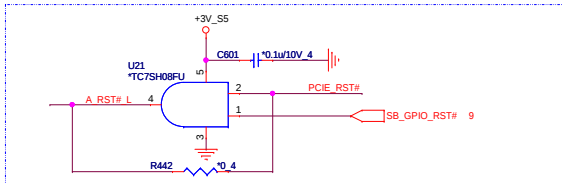
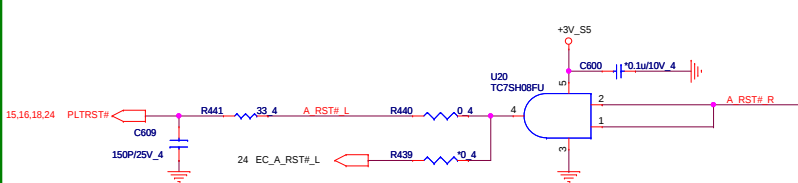
PROJECT : ZQP
Quanta Computer Inc.

Size	Document Number DDR3 SO-DIMM (STD)	Rev 1A
Date:	Monday, February 21, 2011	Sheet 6 of 32



BUS1 A2

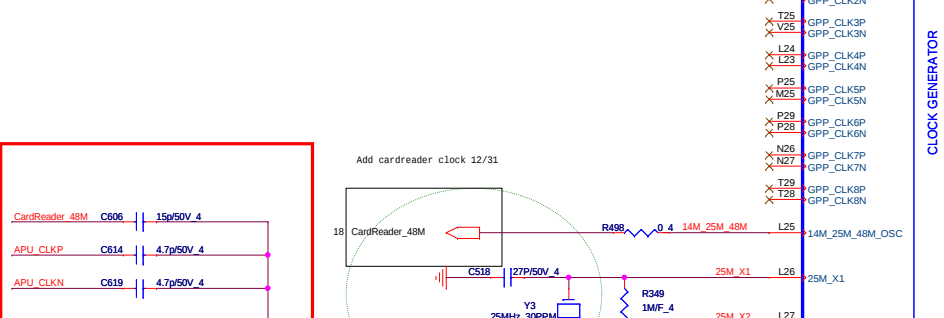
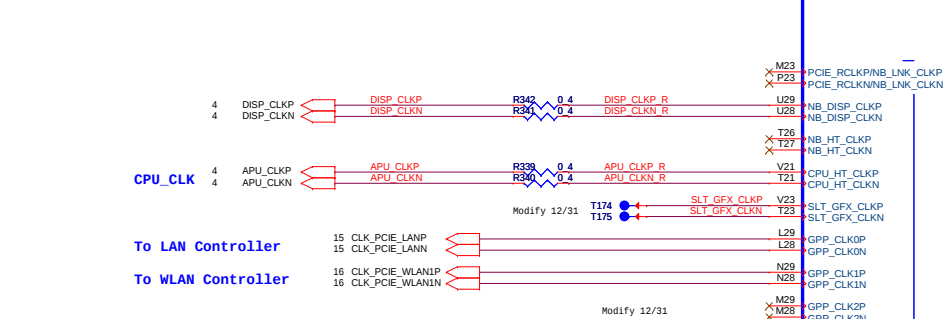
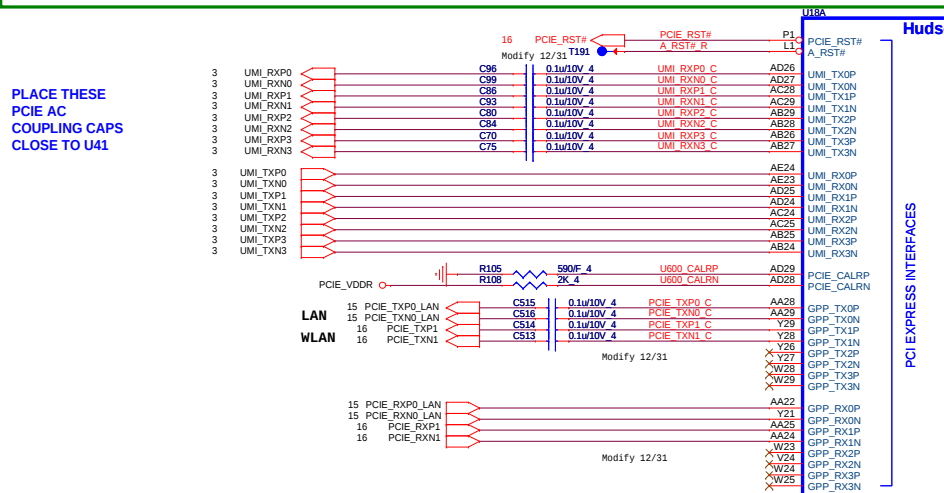
DDR3-DIMM0 H=4 Standard



PCIE_VDD0 11
+3V_55 9,10,11,12,15,21,22,26
+3VPCU 13,22,23,24,25,26,31
+5VPCU 26,27,28,31

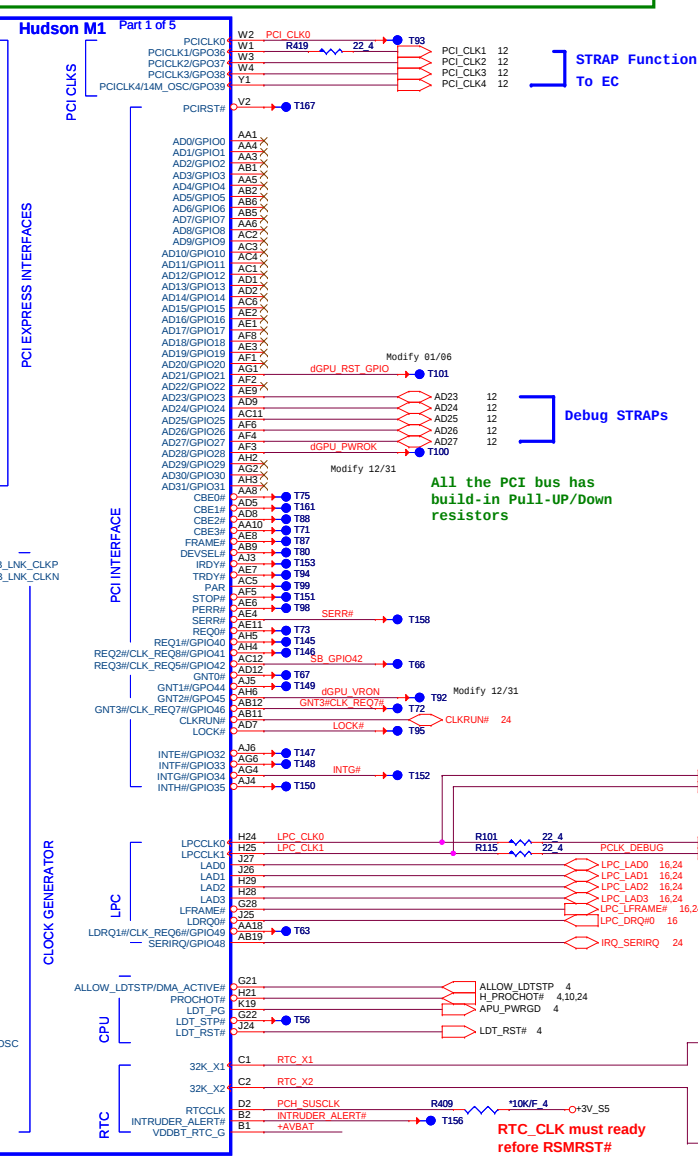
This page is different AMD Nil expect RTC circuit

PLACE THESE
PCIE AC
COUPLING CAPS
CLOSE TO U41



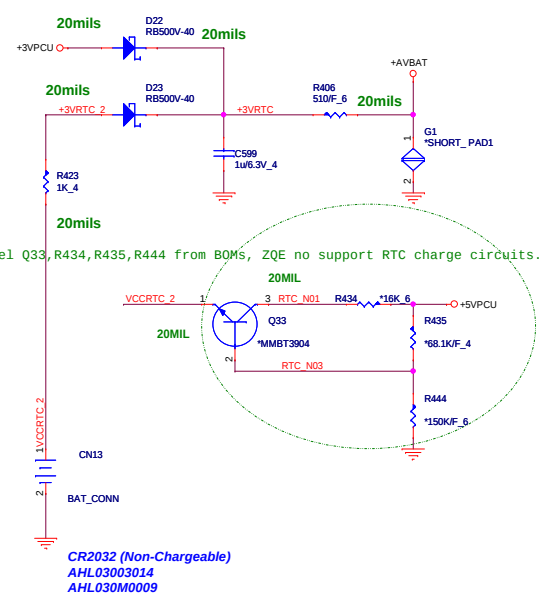
Add C606,C614,C619 for strong clock
02/15 REV:B

BG625000486



INTRUDER_ALERT# Left not connected (Southbridge has 50-kohm internal pull-up to VBAT).

RTC



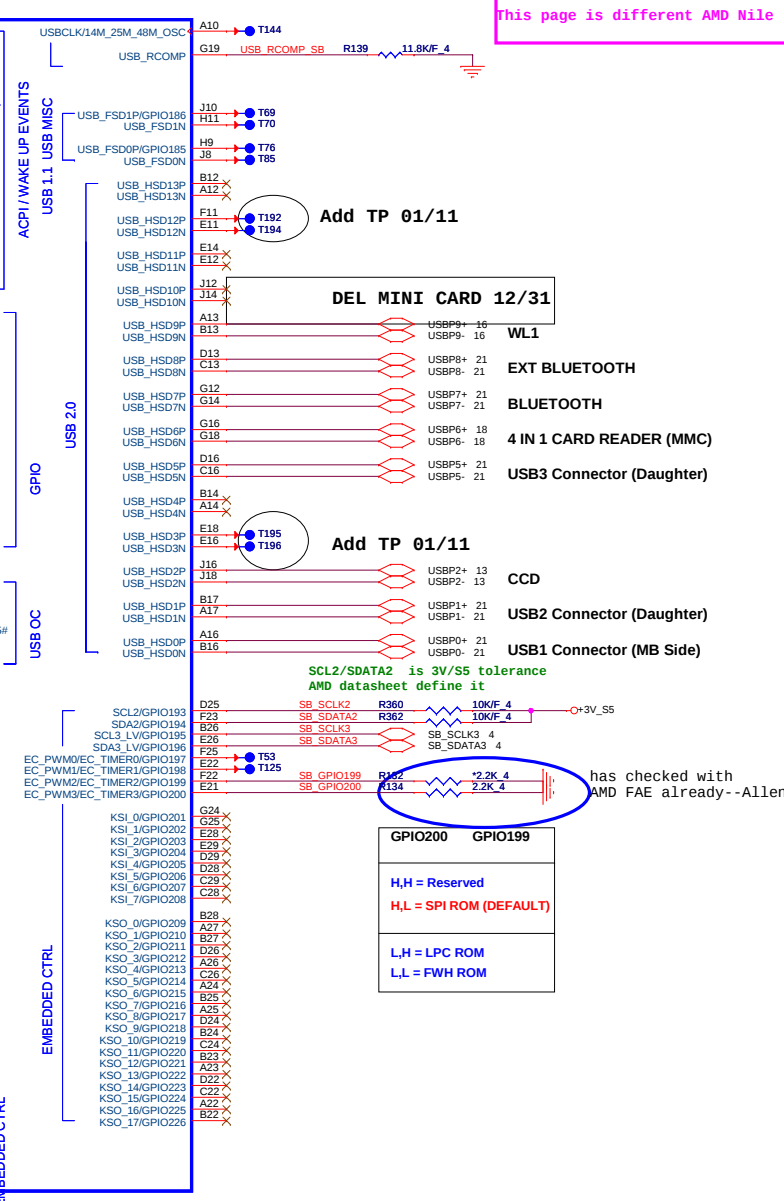
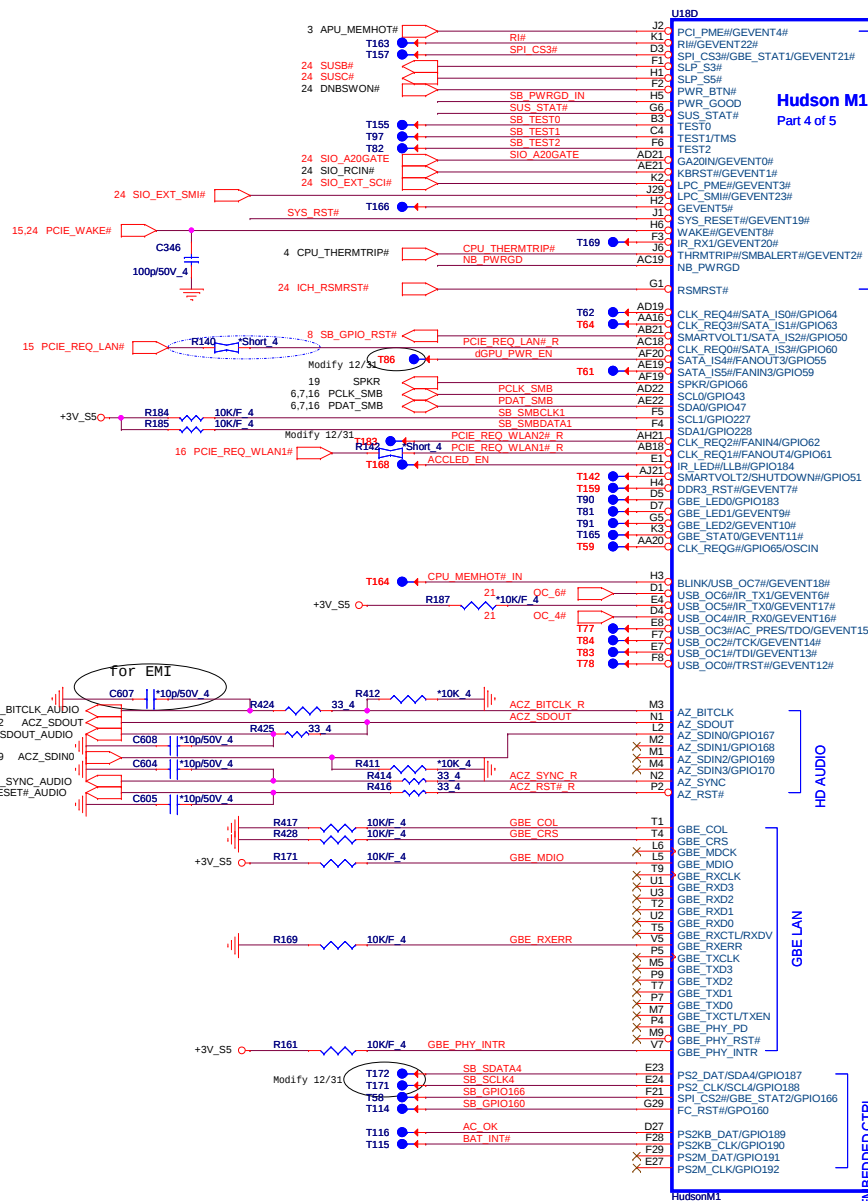
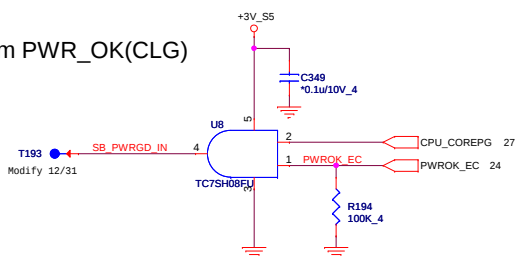
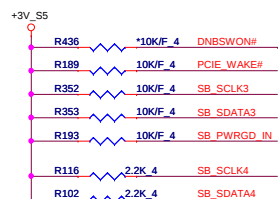
CR2032 (Non-Chargeable)
AHL03003014
AHL030M0009

To STRAPS Page



PROJECT : ZQP
Quanta Computer Inc.

Size	Document Number	Rev
	Hudson PCIe/LPC/CPU IF(U5)	1A
Date:	Monday, February 21, 2011	Sheet 8 of 32



GPIO200	GPIO199
H,H = Reserved	H,L = SPI ROM (DEFAULT)
L,H = LPC ROM	L,L = FWH ROM

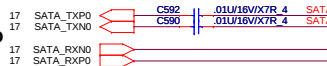
has checked with
AMD EAE already--Allen



SATA PORT 0,1,2,3
can support AHCI
mode

PLACE SATA AC COUPLING
CAPS CLOSE TO HUDSON M1

SATA HDD

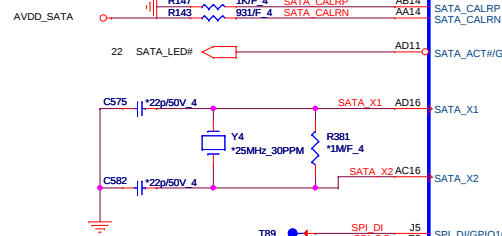


SATA ODD



PLACE SATA CAL RES
VERY CLOSE TO BALL
OF HUDSON M1

XTLVDD_SATA-- SATA
crystal power
PLVDD_SATA-- SATA
PLL
POWER



U1B8
Hudson M1
Part 2 of 5

SERIAL ATA

HW MONITOR

SPI ROM

Hudson M1
Part 2 of 5

FLASH

W5

W6

W7

W8

B6

A5

B5

C7

A3

B4

A4

C5

A7

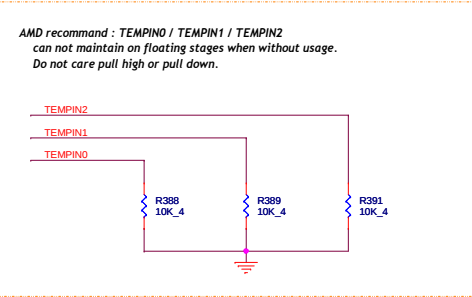
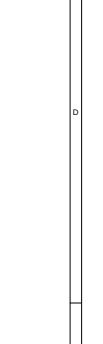
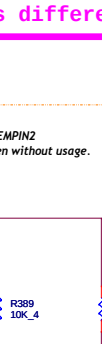
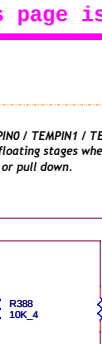
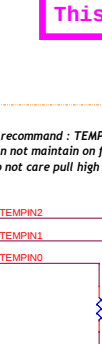
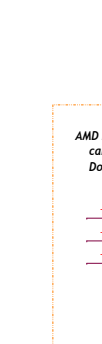
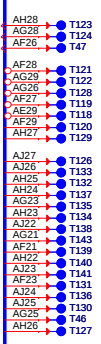
B7

B8

A8

G27

Y2



0831--modify location

MB ID

CPU THERMAL	GPIO52
External	1
SB-TSI	0

SB8XX Hold Time	GPIO53
1.2V	1
1.1V	0

DU1/MK2	GPIO56
MK2.0 AMD	1
DU1.0 AMD	0

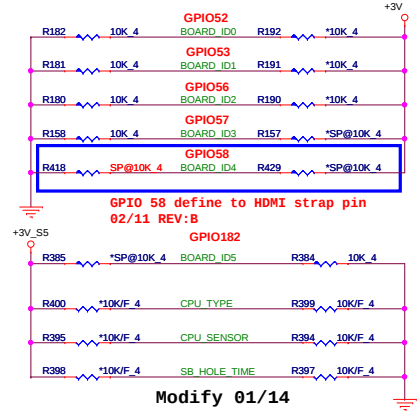
(Dis) SW	GPIO57
UMA	0

With HDMI	GPIO58
Without HDMI	0

PX4.0	GPIO182
PX3.0	0

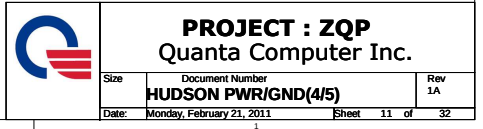


0831--add circuit



Modify 01/14

PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.

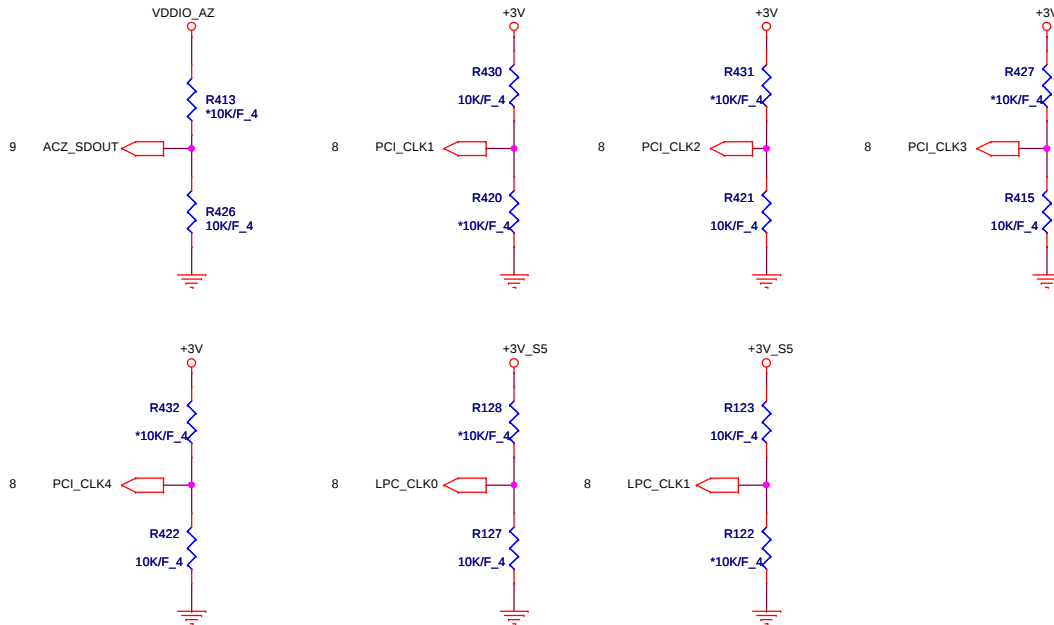




OVERLAP COMMON PADS WHERE
POSSIBLE FOR DUAL-OP RESISTORS.

REQUIRED STRAPS

internal have pull
Hi 10K, confirm AMD
ward this pull Hi
not need



PCI_CLK4 CPU/NB HT Clock Selection
0 V - Reserved.
3.3 V - Required setting for integrated clock mode.
This strap is not used if the strap CLKGEN is
configured for external clock generator mode.

REQUIRED STRAPS

	AZ_SDOUT	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	GPIO200	GPIO199
PULL HIGH	LOW POWER MODE	ALLOW PCIE Gen2 DEFAULT	Watchdog Timer Enabled	USE DEBUG STRAP	non_Fusion CLOCK MODE	EC ENABLED	CLKGEN ENABLED DEFAULT	H,H = Reserved H,L = SPI ROM (Default)	
PULL LOW	PERFORMANCE MODE DEFAULT	FORCE PCIE Gen1	Watchdog Timer Disabled DEFAULT	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLED	L,H = LPC ROM L,L = FWH ROM	

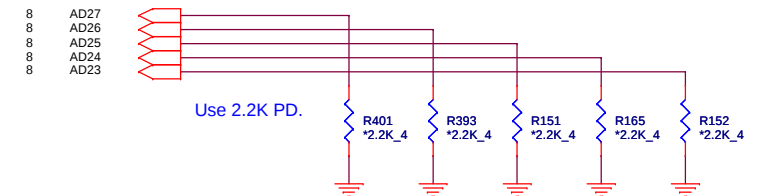


VDDIO_AZ 11
+3V 4,5,6,7,9,10,11,13,14,16,18,19,22,23,24,26,27,28,29,30,31
+3V_S5 8,9,10,11,15,21,22,26

12

DEBUG STRAPS

HUDSON-M1 HAS 15K INTERNAL PU FOR PCI_AD[27:23]



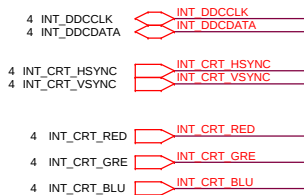
	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT



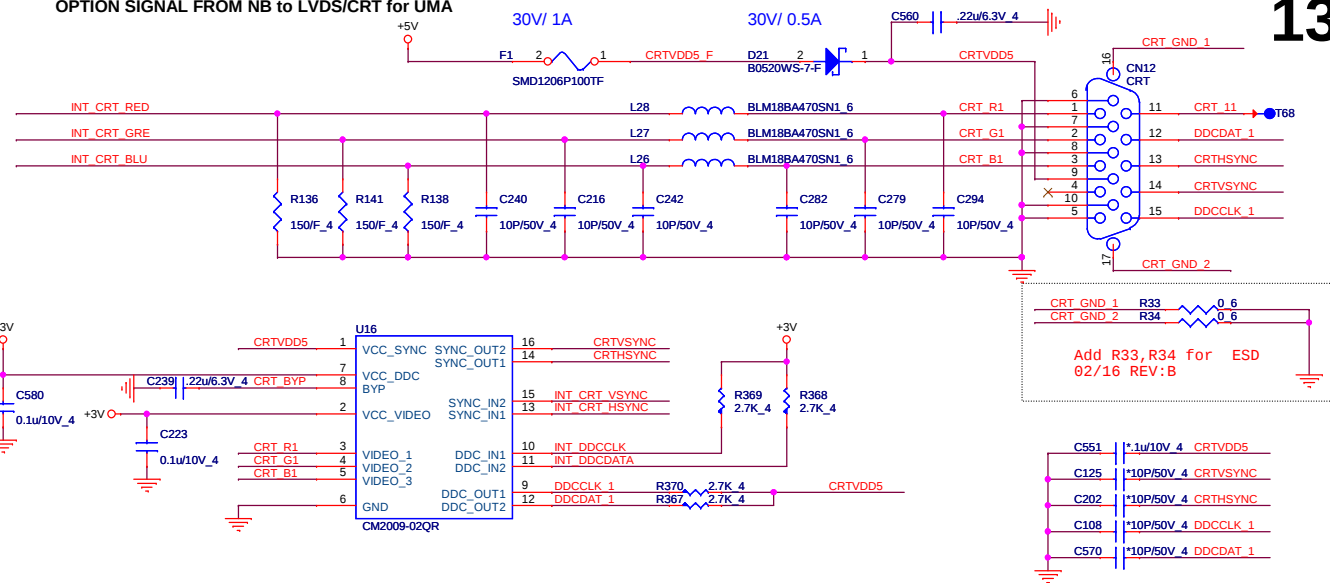
PROJECT : ZQP
Quanta Computer Inc.

Size	Document Number	Rev
	HUDSON STRAPS/PWRGD(5/5)	1A
Date:	Monday, February 21, 2011	Sheet 12 of 32

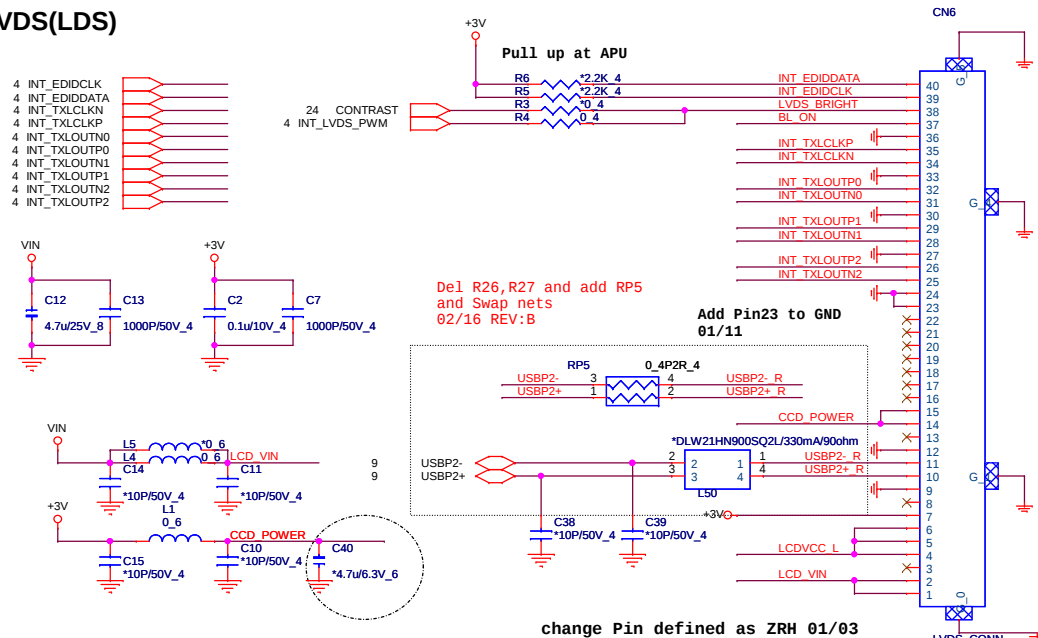
CRT



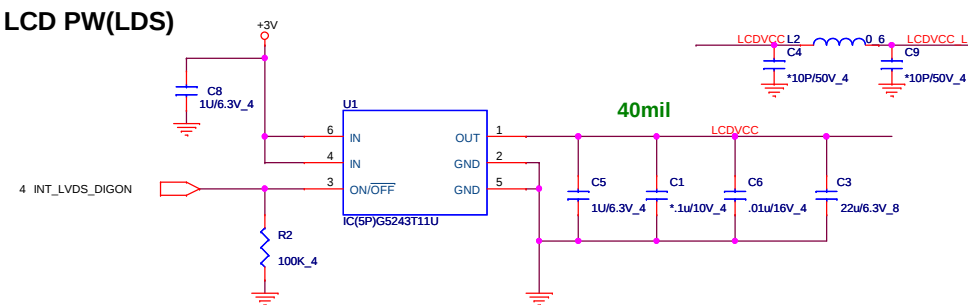
OPTION SIGNAL FROM NB to LVDS/CRT for UMA



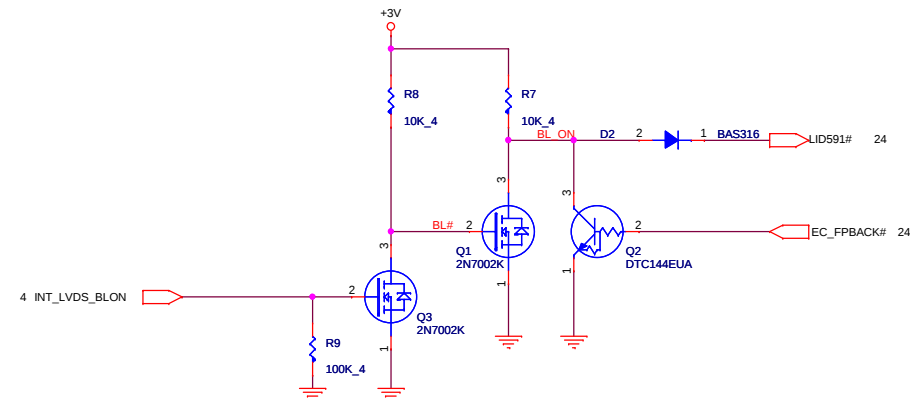
LVDS(LDS)



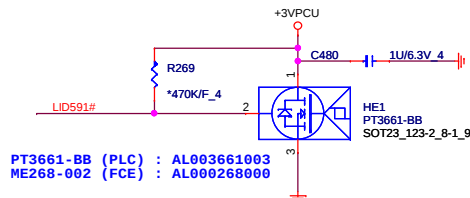
LCD PW(LDS)



Backlight Control(LDS)



Lid Switch (HSR)



PROJECT : ZQP
Quanta Computer Inc.

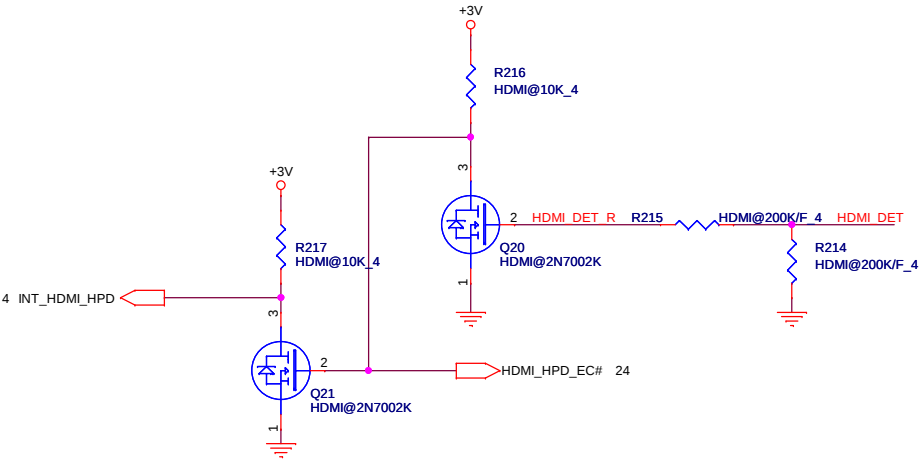
Size	Document Number	Rev
	CRT/LVDS/LID	1A
Date:	Monday, February 21, 2011	Sheet 13 of 32

HDMI SDVO I2C Control



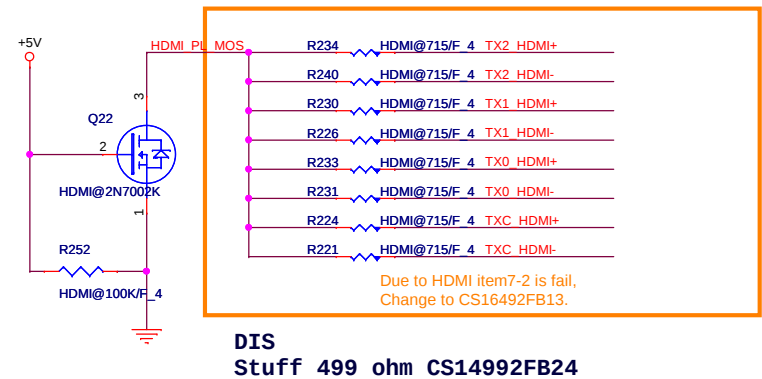
HDMI HPD SENSE (HDM)

UMA use +3V for the detect pin
Dis use +3V_DELAY for the detect pin



HDMI (HDM)

Close to HDMI Connector

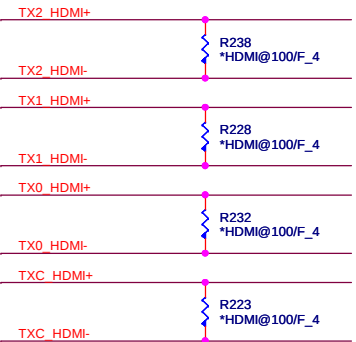


DIS
Stuff 499 ohm CS14992FB24



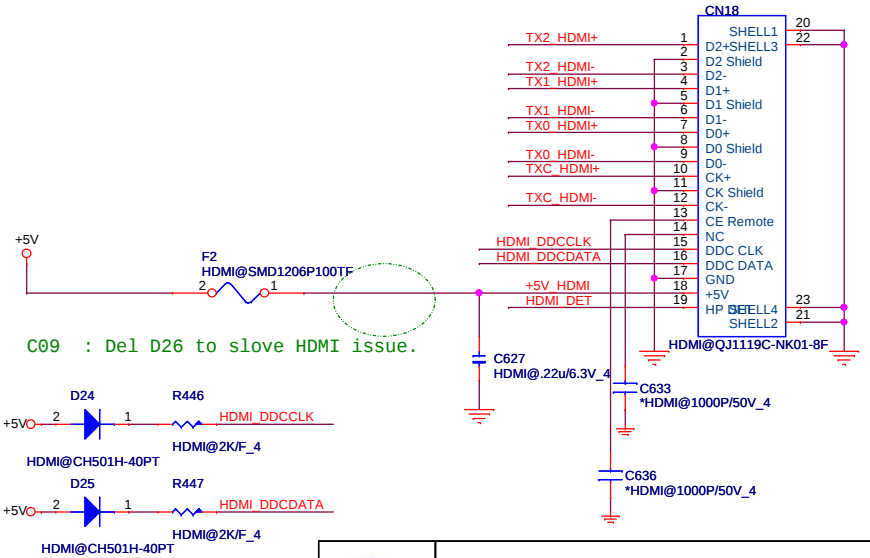
EMI reserve for HDMI(EMC)

Close connector



Added HDMI function
01/19 REV:B

HDMI PORT (HDM)



C09 : Del D26 to slove HDMI issue.



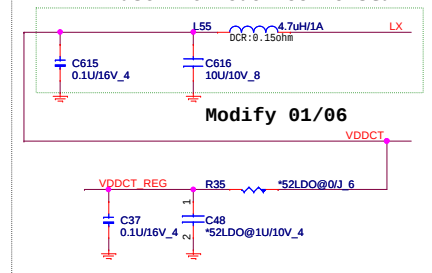
PROJECT : ZQP
Quanta Computer Inc.

Size	Document Number	Rev
	HDMI	1A
Date:	Monday, February 21, 2011	Sheet 14 of 32

<BOM note>
If center tap power come from internal switch regulator
=>Stuff 52SWR@ (Default)
If center tap power come from internal LDO
=>Stuff 52LDO@

<Layout note>
Close to Pin1

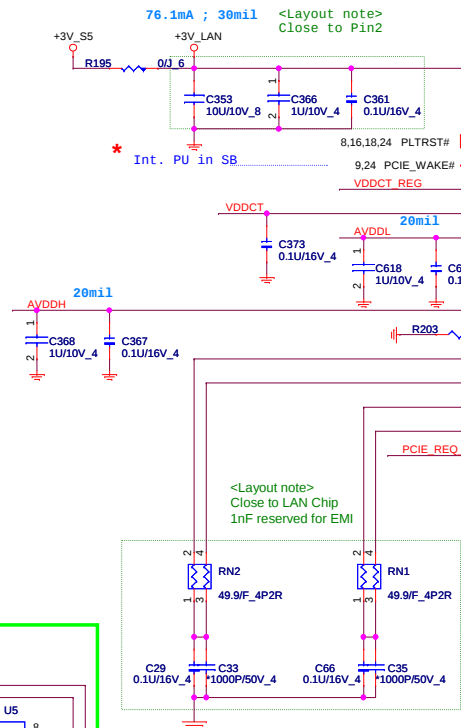
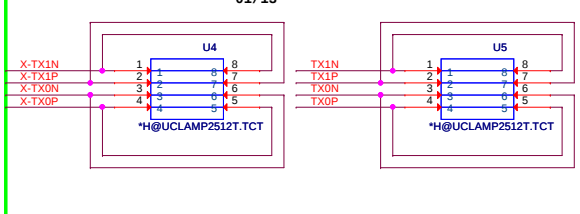
If use LDO mode L55 no stuff



Modify 01/06

BG625000486

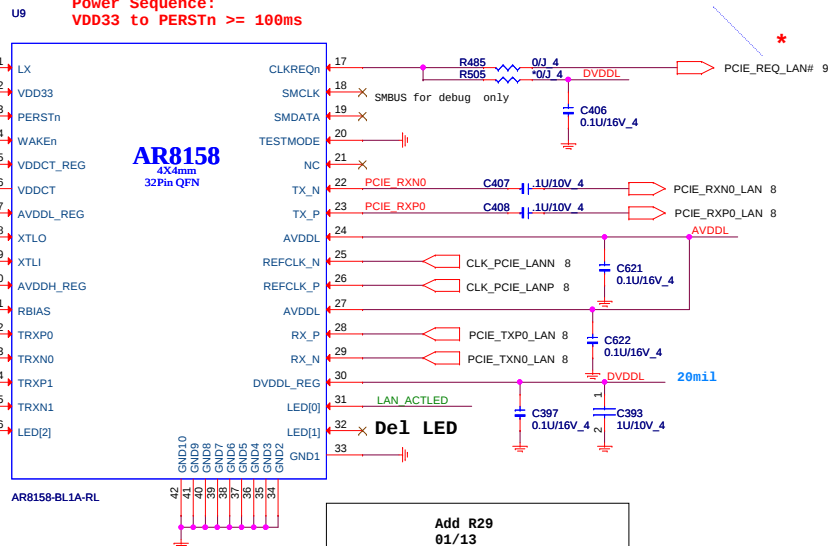
Add R28/D4 for 家電下鄉
01/13



* Why does Pin17 CLKREQn connect to Pin16(LED2) and Pin30(DVDDL)?

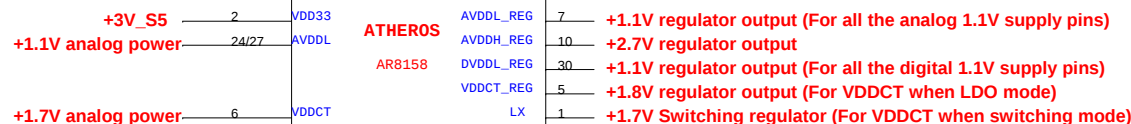
Power Sequence:
VDD33 to PERSTn >= 100ms

PU in CLK Gen.



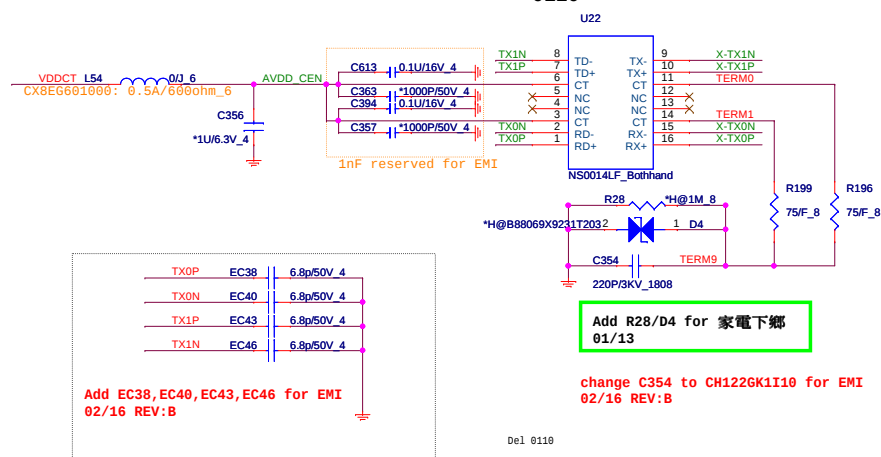
Add R29
01/13

R29 5.1K/0.8 LAN ACTLED
Active LED Pin:
Non-overclocking=>active high



TRANSFORMER (LAN)

exchange pair 0/1
0110



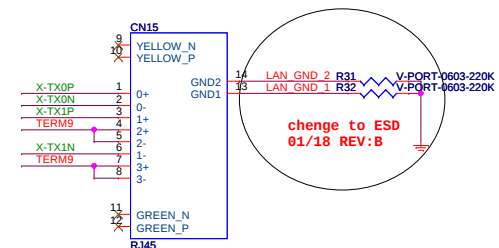
Add R28/D4 for 家電下鄉
01/13

change C354 to CH1226K110 for EMI
02/16 REV:B

Del 0110

RJ45 Connector (LAN)

Del LAN LED 01/05



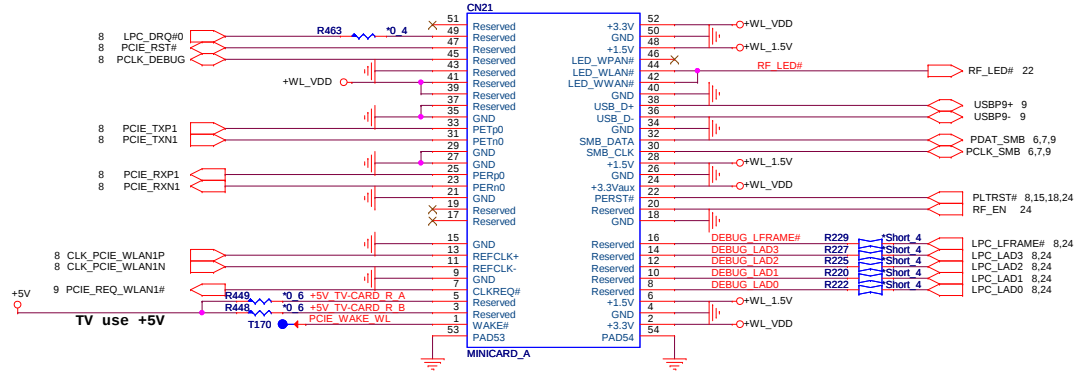
We will change RJ45 connector

PROJECT : ZQP Quanta Computer Inc.		
Size	Document Number	Rev
	LAN AR8158L	1A
Date:	Monday, February 21, 2011	Sheet 15 of 32

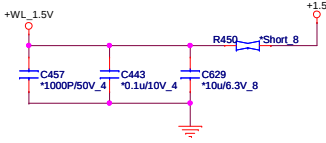
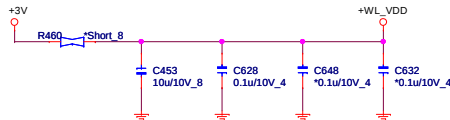
MINI-CARD WLAN(MPC)

+3.3V: 1000mA
+3.3Vaux:330mA
+1.5V:500mA

Check LED signal. (active high or low)



Debug



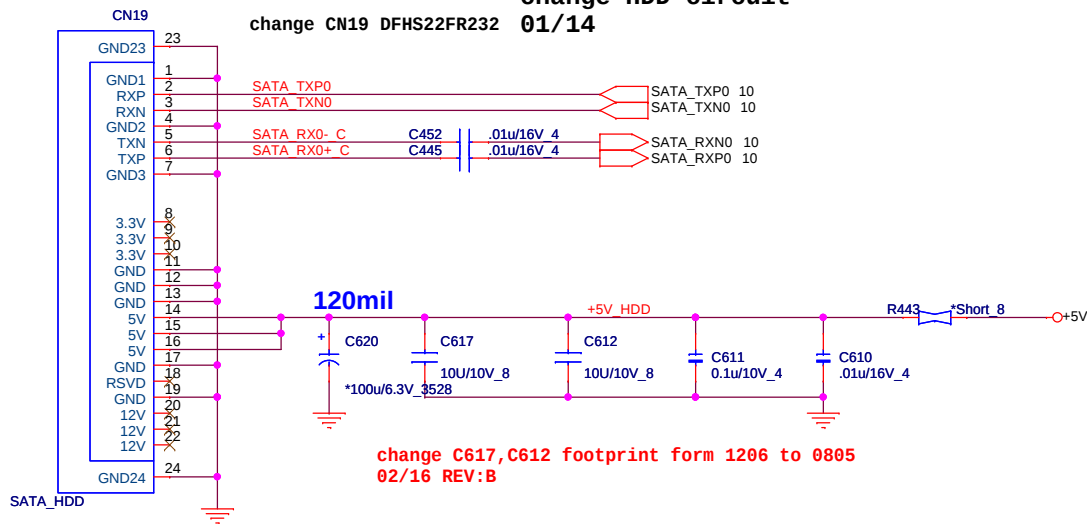
PROJECT : ZQP
Quanta Computer Inc.

Size	Document Number	Rev
	MINI PCI-E card	1A
Date:	Monday, February 21, 2011	Sheet 16 of 32

SATA HDD

change HDD circuit

change CN19 DFHS22FR232 01/14

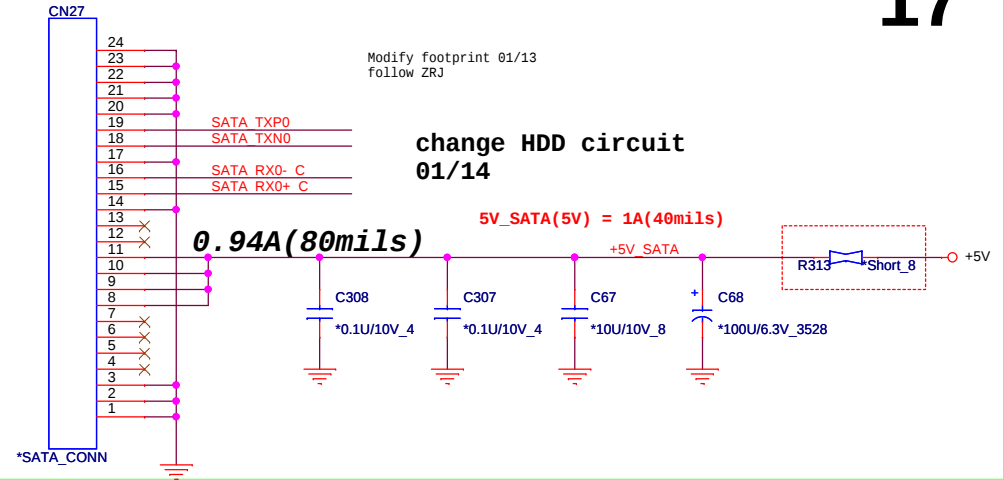


SATA HDD(HDD)

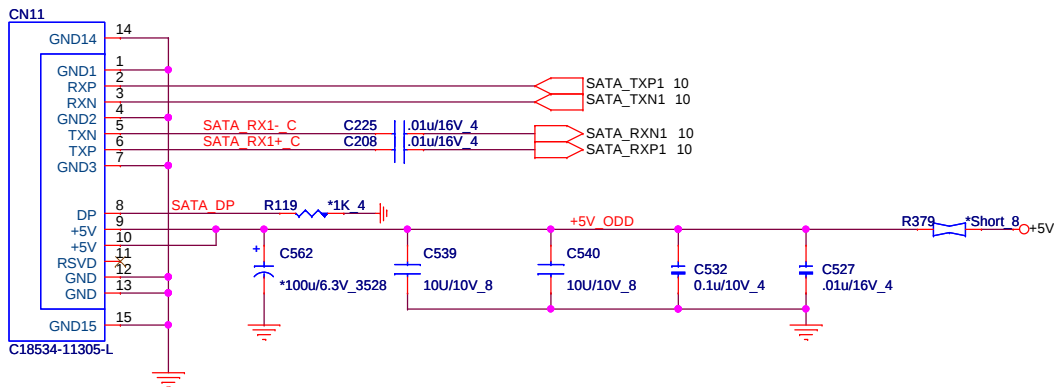
17

Modify footprint 01/13
follow ZRJ

change HDD circuit
01/14



SATA ODD

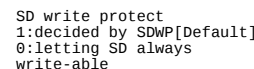


change C539,C552 footprint form 1206 to 0805
02/16 REV:B

			PROJECT : ZQP Quanta Computer Inc.	
Size	Document Number		Rev	
	SATA-HDD/ODD/HOLE		1A	
Date:	Monday, February 21, 2011	Sheet	17 of	32

18

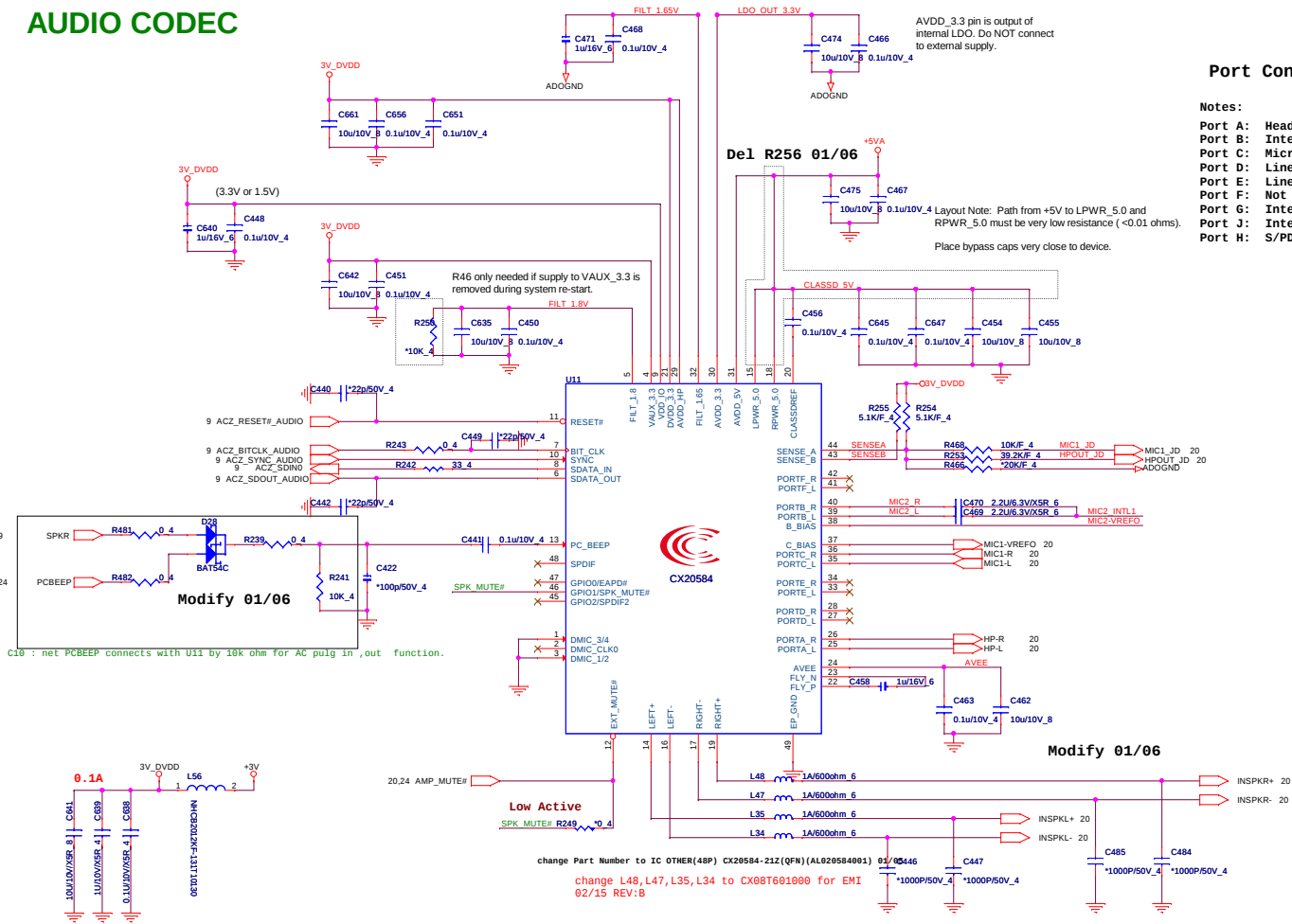
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Port Configuration

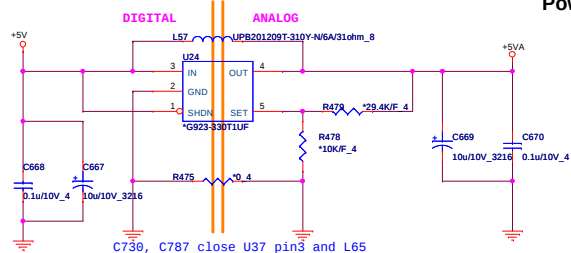
Notes:

- Port A: Headphone jack (jack shared with S/PDIF)
 Port B: Internal MIC (mono or stereo)
 Port C: Microphone/LI/L0 jack
 Port D: Line Out jack (Optional)
 Port E: Line In jack (Optional)
 Port F: Not used.
 Port G: Internal stereo speakers
 Port J: Internal stereo digital mic (Optional)
 Port H: S/PDIF (jack shared with headphone)

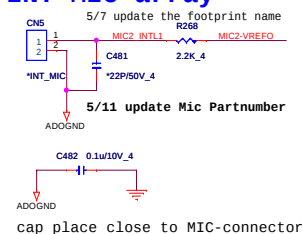


1. The VDD_IO and VAUX_3.3 pins should be connected to same power supply domain as HDA bus controller so that the HDA controller and codec bus interface will power-up at the same time. This will avoid bus leakage issues if using HDA controller with bus pull-up strap options. See other FET option on this page if these supplies are not on same domain as HDA controller.
2. To support Wake-on-Jack, the codec VAUX_3.3 pin must be powered from a Standby supply.
3. C309, C310, C311 are optional. Do not install unless needed for EMI/SI.

Power (ADO)



INT MIC array



PROJECT : ZQP
Quanta Computer Inc.

Size	Document Number	Rev
	CONEXANT 20584	1A
Date:	Monday, February 21, 2011	Sheet 19 of 32

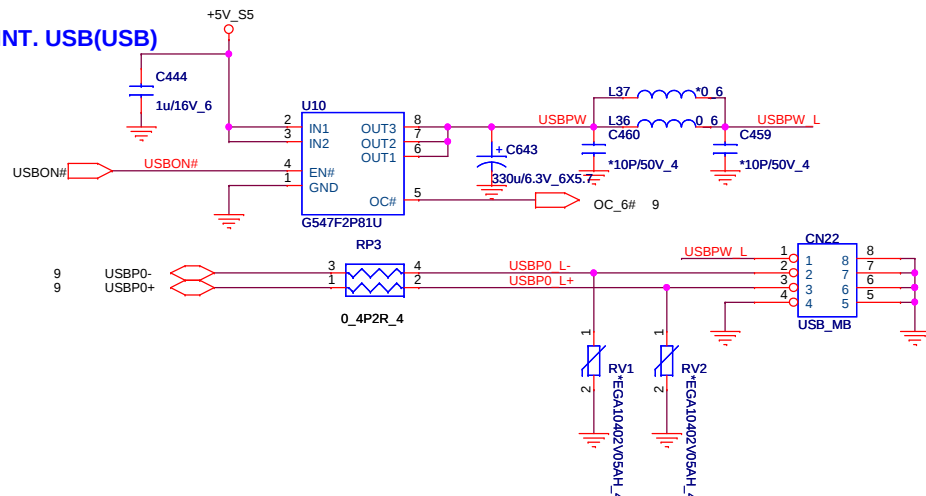
A



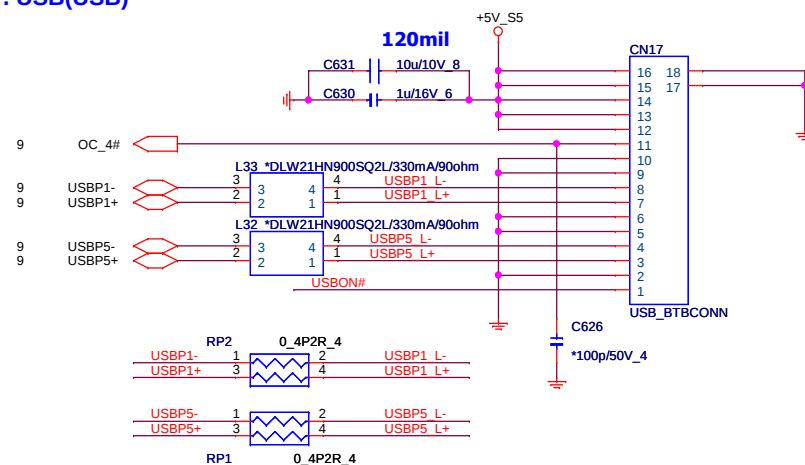
A



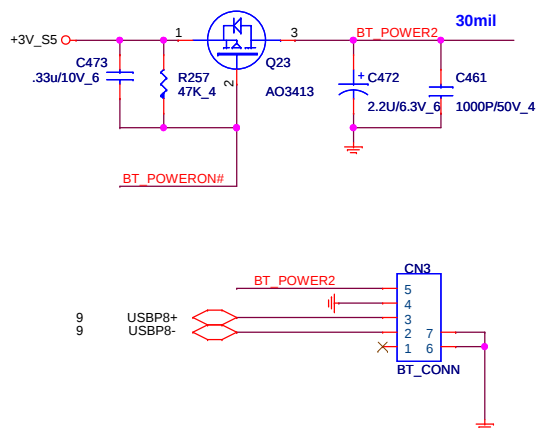
INT. USB(USB)



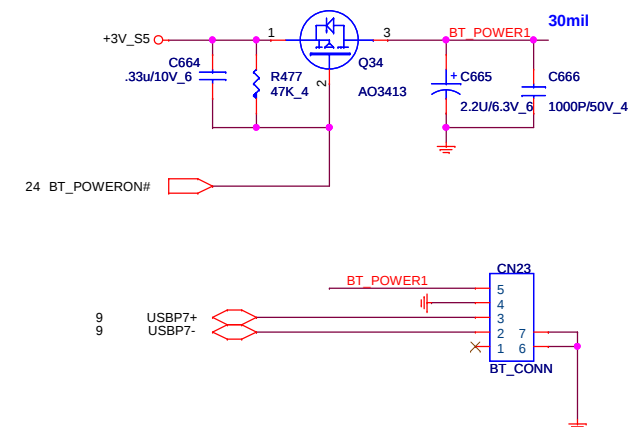
EXT. USB(USB)



BLUETOOTH V2.1 CONN(BTM)



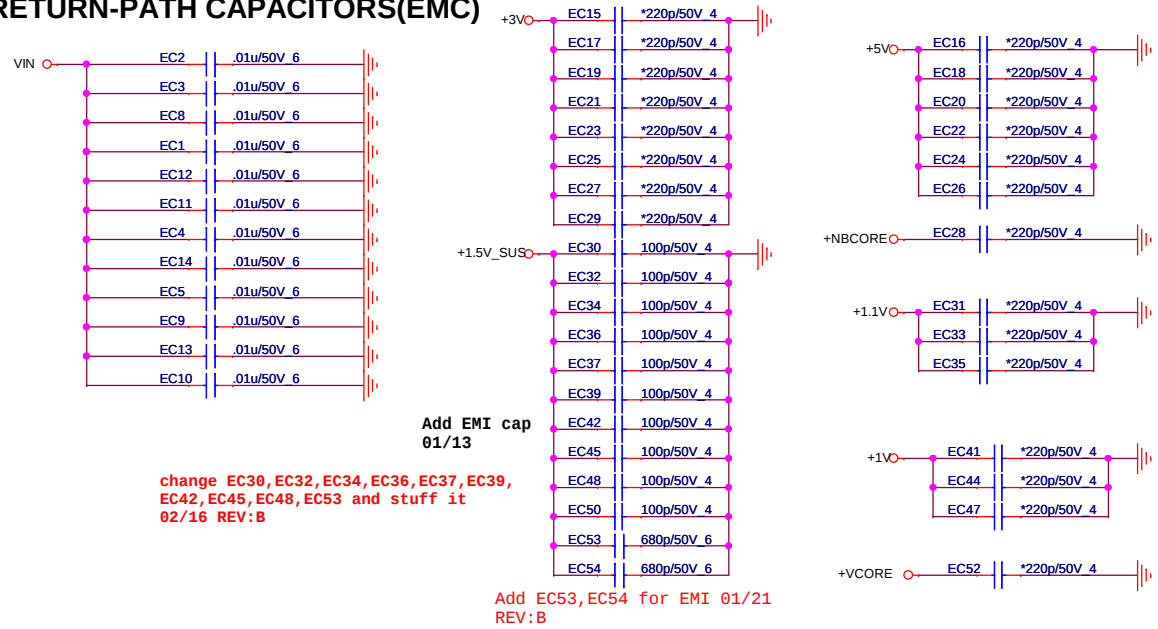
BLUETOOTH V3.0 CONN(BTM)



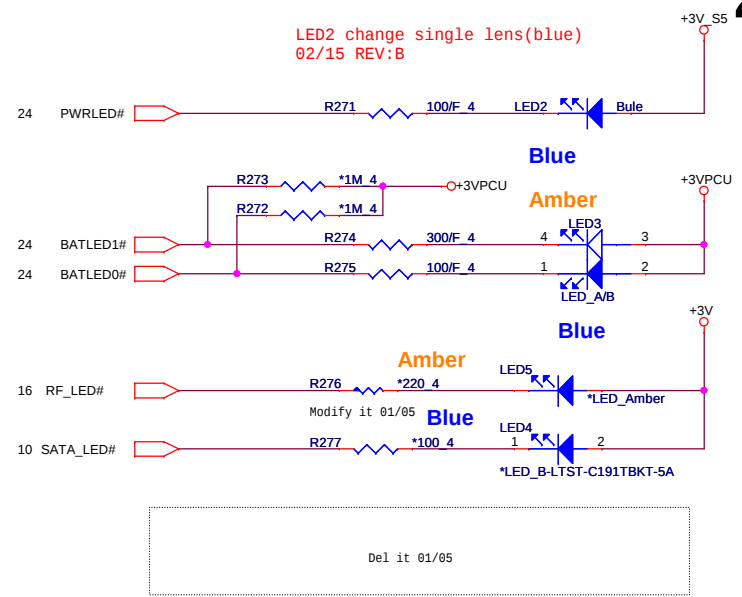
PROJECT : ZQP
Quanta Computer Inc.

Size	Document Number	Rev
	USB/BT	1A
Date:	Monday, February 21, 2011	Sheet 21 of 32

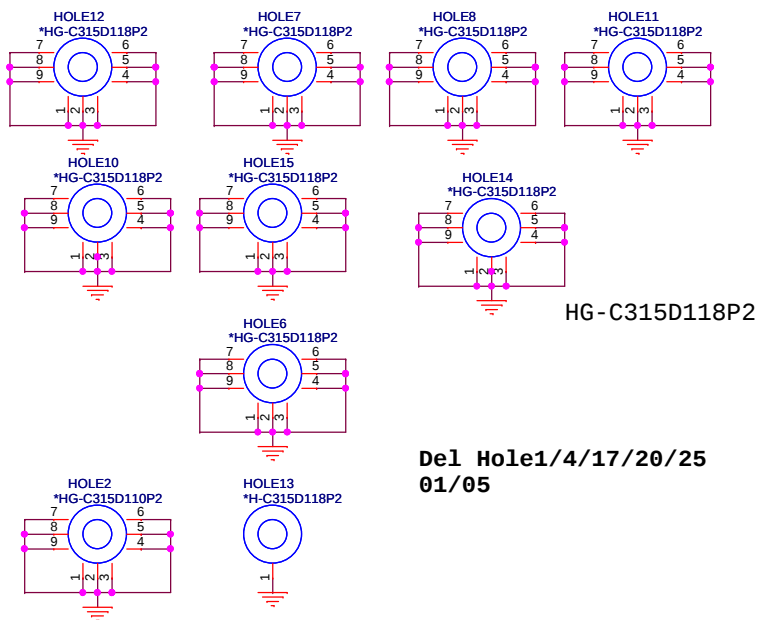
EE RETURN-PATH CAPACITORS(EMC)



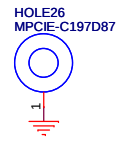
LED(UIF)



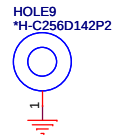
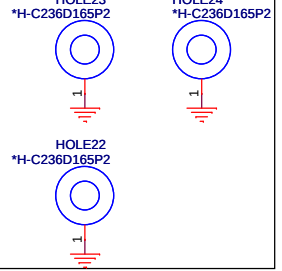
HOLE(OTH)



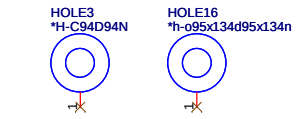
mini PCI



cpu



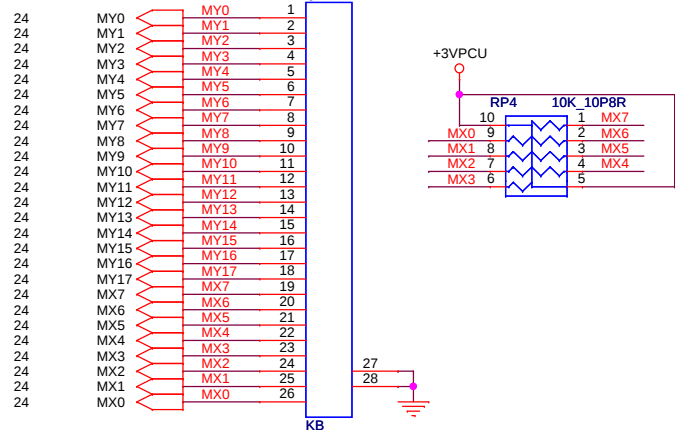
No stuff HOLE9 REV:B 02/17



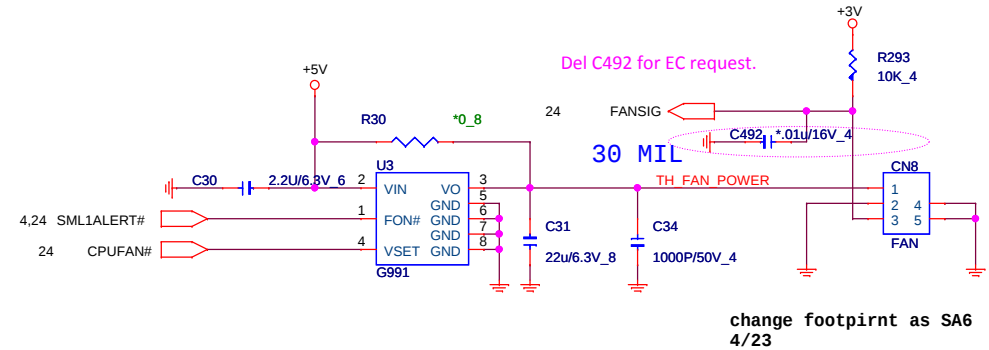
CPU nut PN : FBBU1001010 x 3 @ SHOLE1~3

		PROJECT : ZQP Quanta Computer Inc.			
Size	Document Number			Rev 1A	
	LED/ EMI/ Screw Hole& Nut				
Date:	Monday, February 21, 2011		Sheet	22 of	32

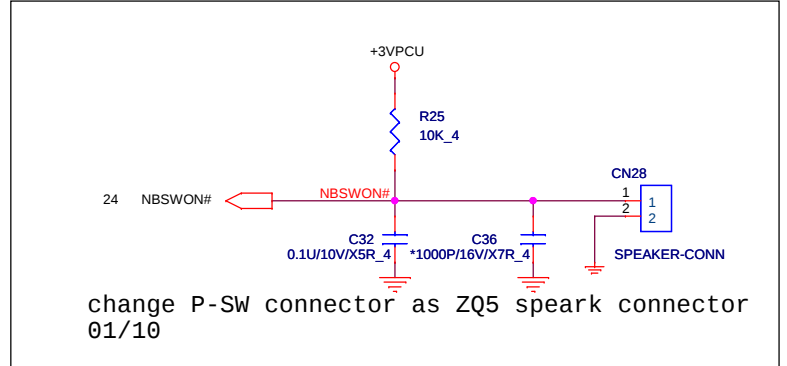
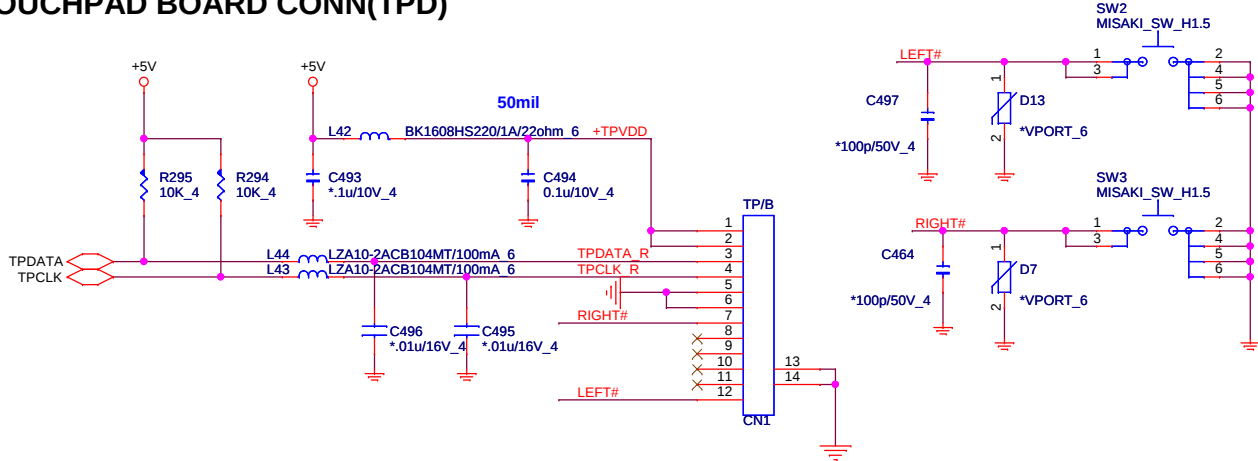
K/B(KBC)



CPU FAN(THM)



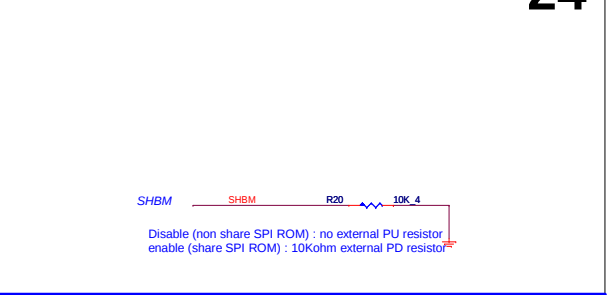
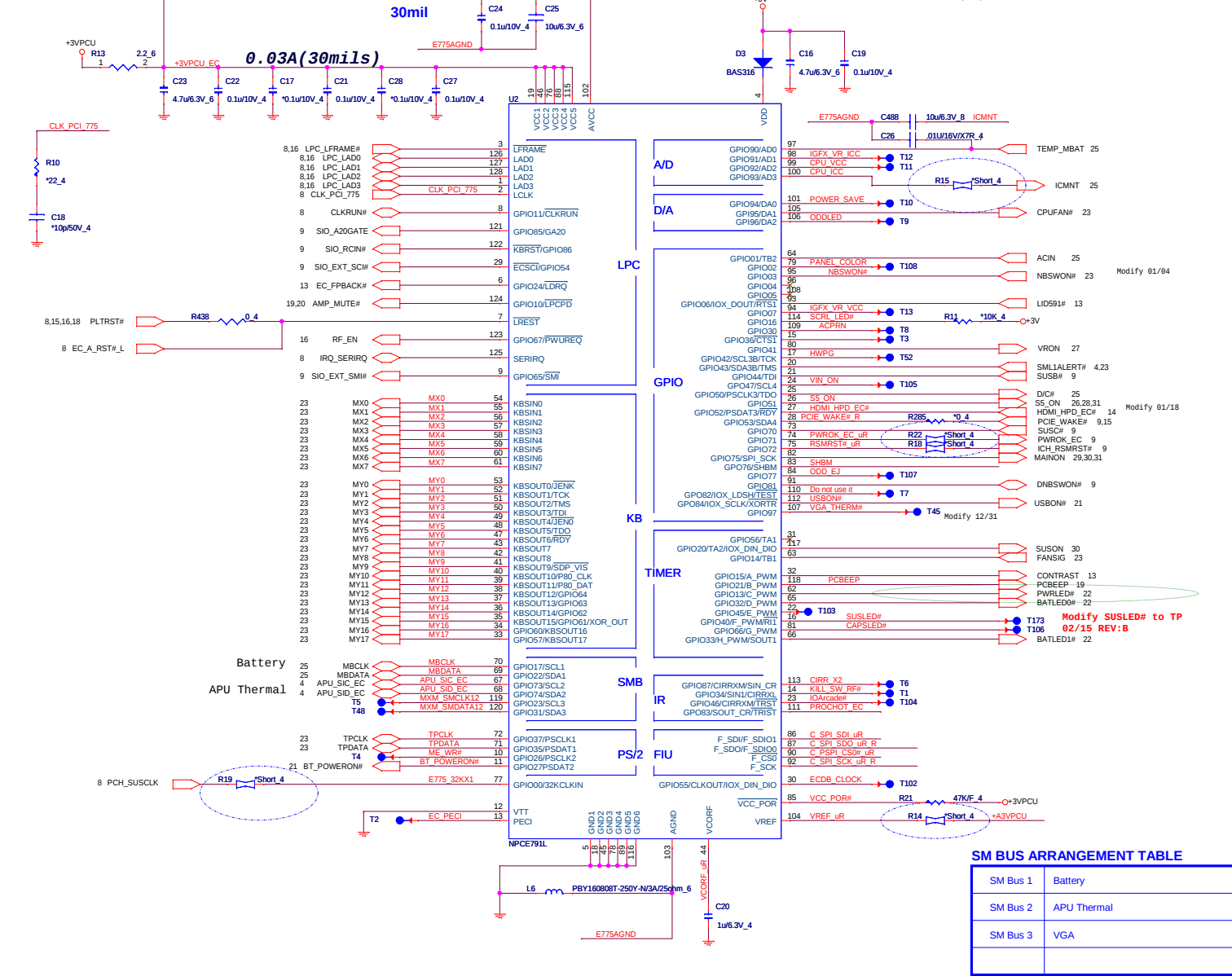
TOUCHPAD BOARD CONN(TPD)



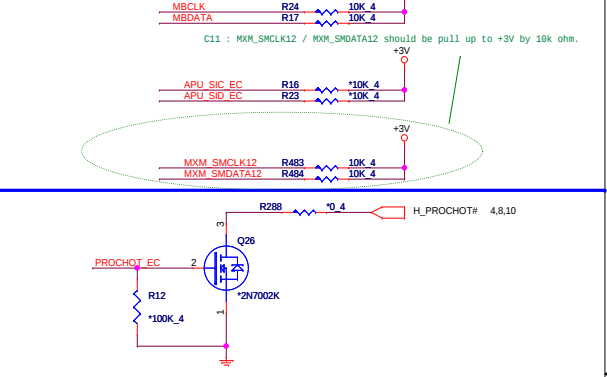
DFFC12FR234 will be EOL by PDC , so change PN to DFFC12FR026

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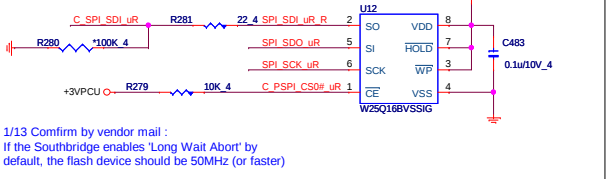
Size	Document Number	Rev
	KB/TP/FAN	1A
Date:	Monday, February 21, 2011	Sheet 23 of 32



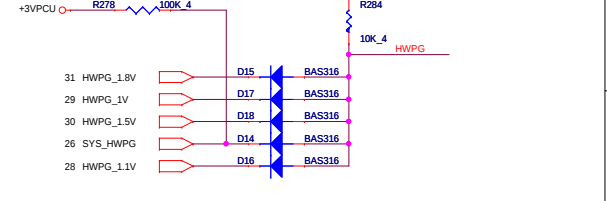
SM BUS PU(KBC)



SPI FLASH(KBC)



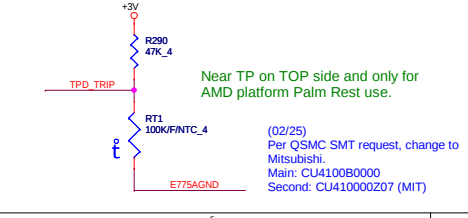
HWPG(KBC)



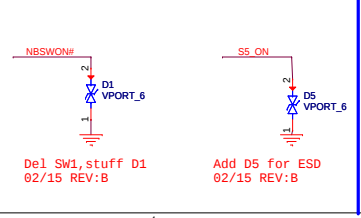
SM BUS ARRANGEMENT TABLE

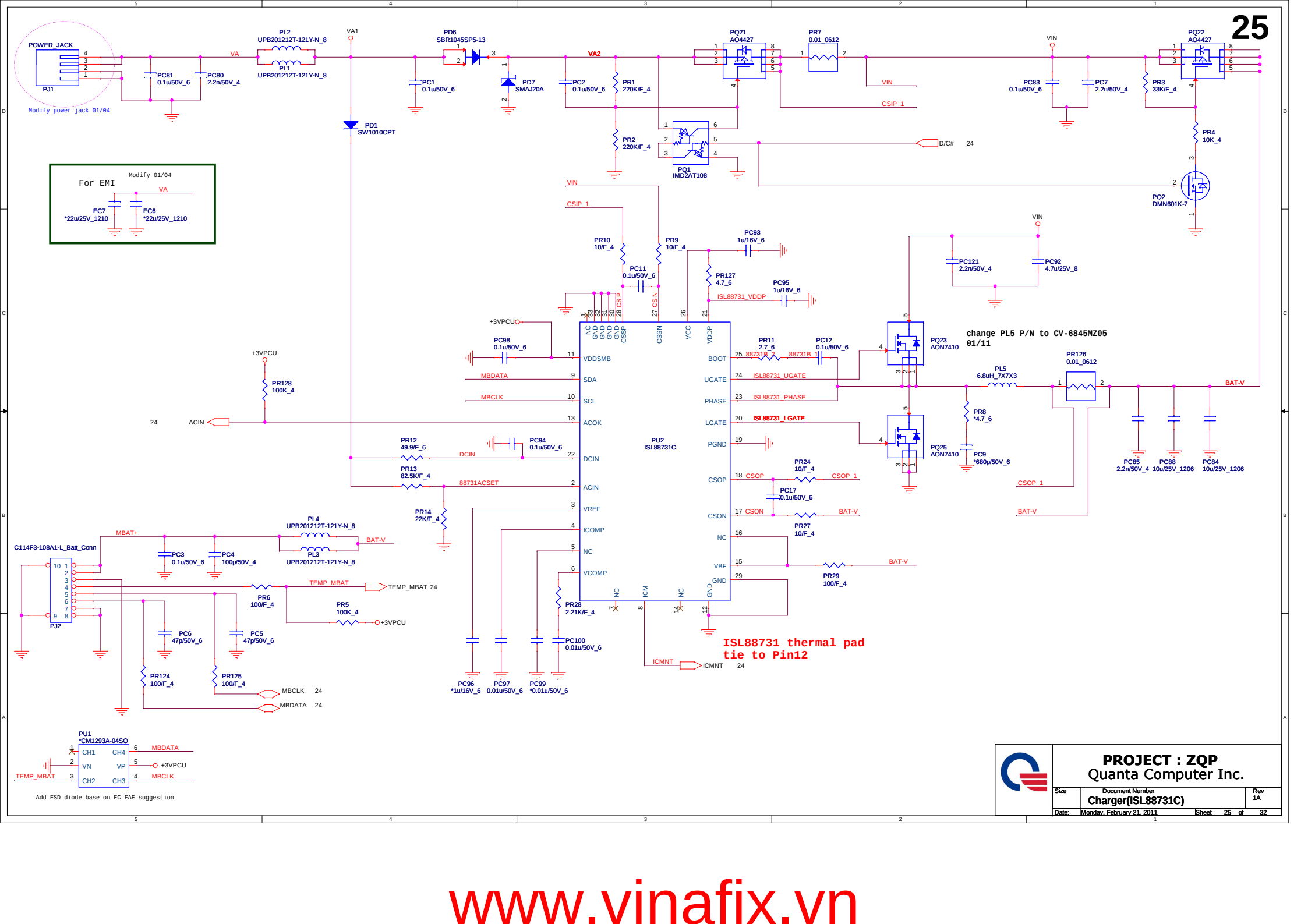
SM Bus 1	Battery
SM Bus 2	APU Thermal
SM Bus 3	VGA

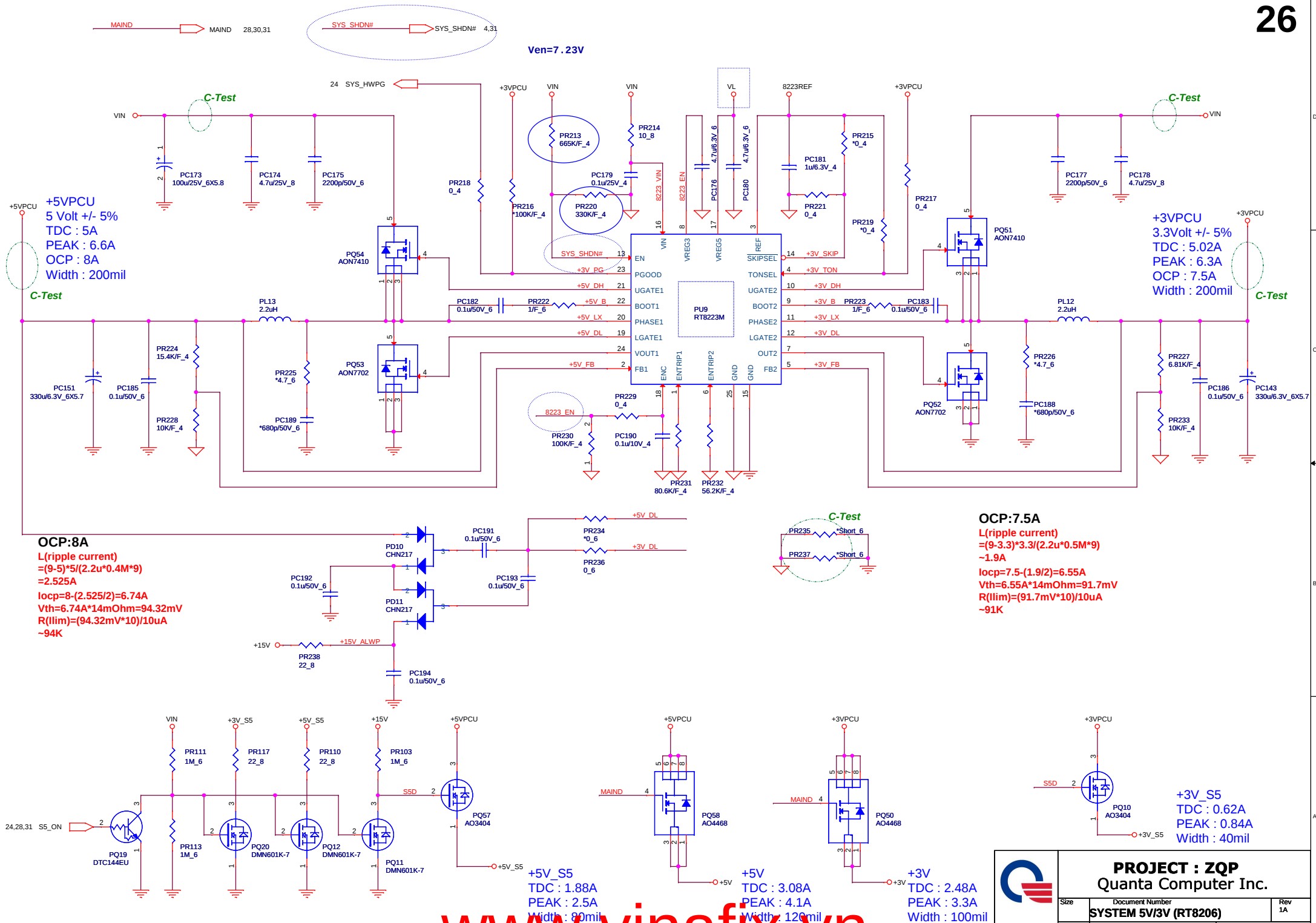
PALM REST THERMAL SENSOR (THM)

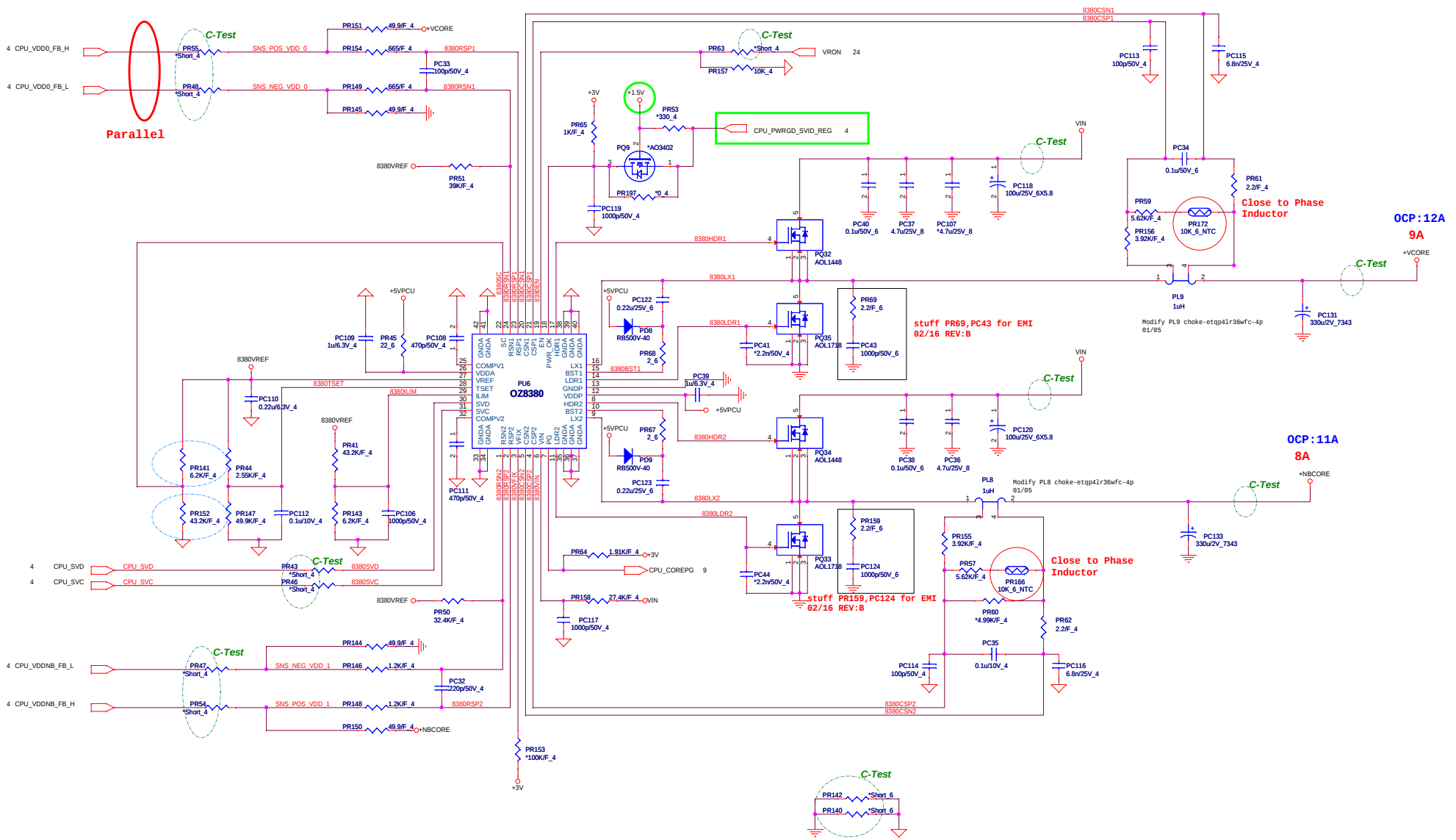


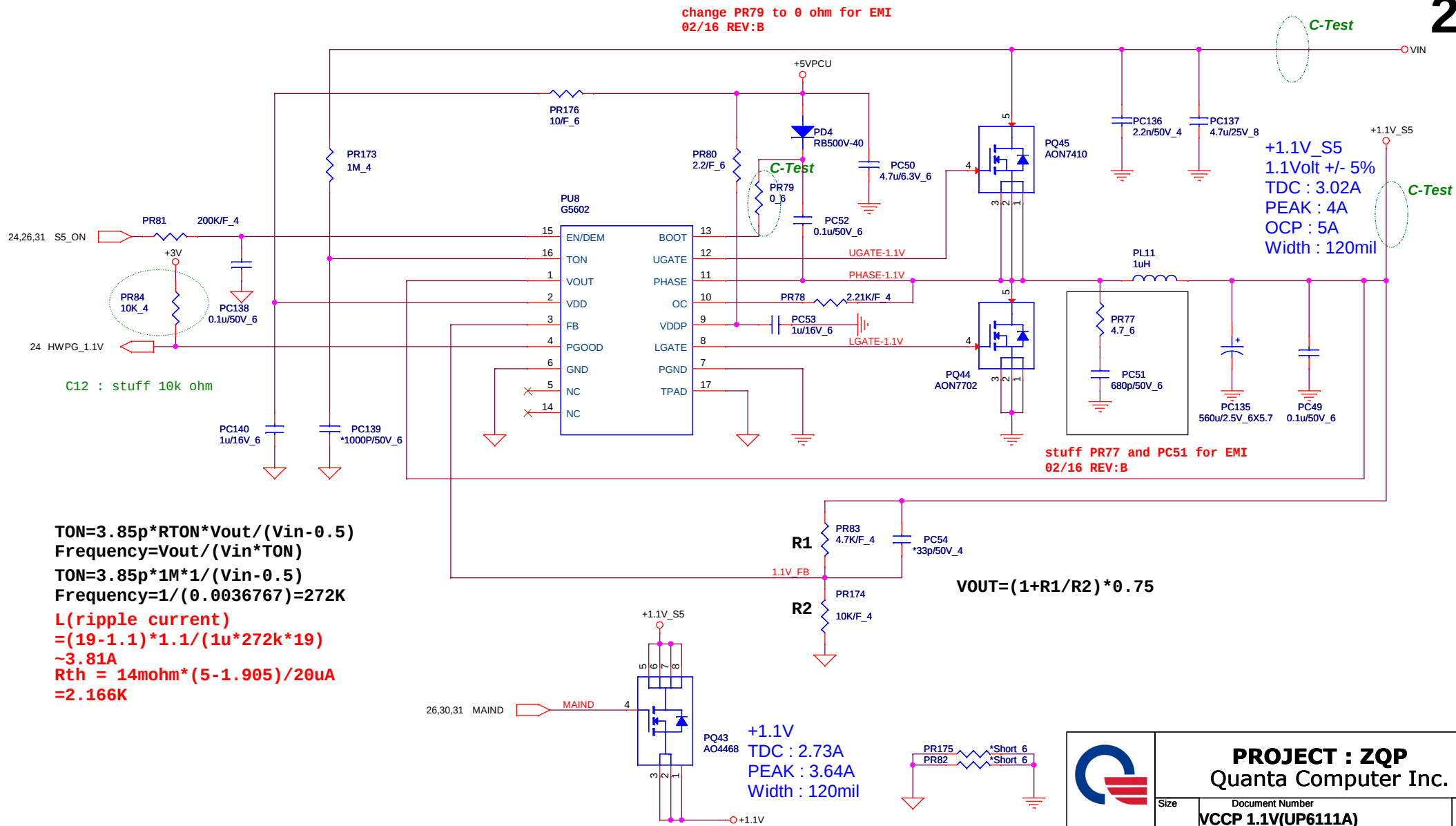
POWER-ON SWITCH (KBC)





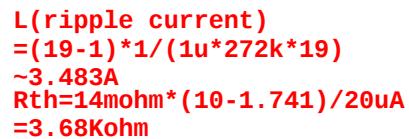






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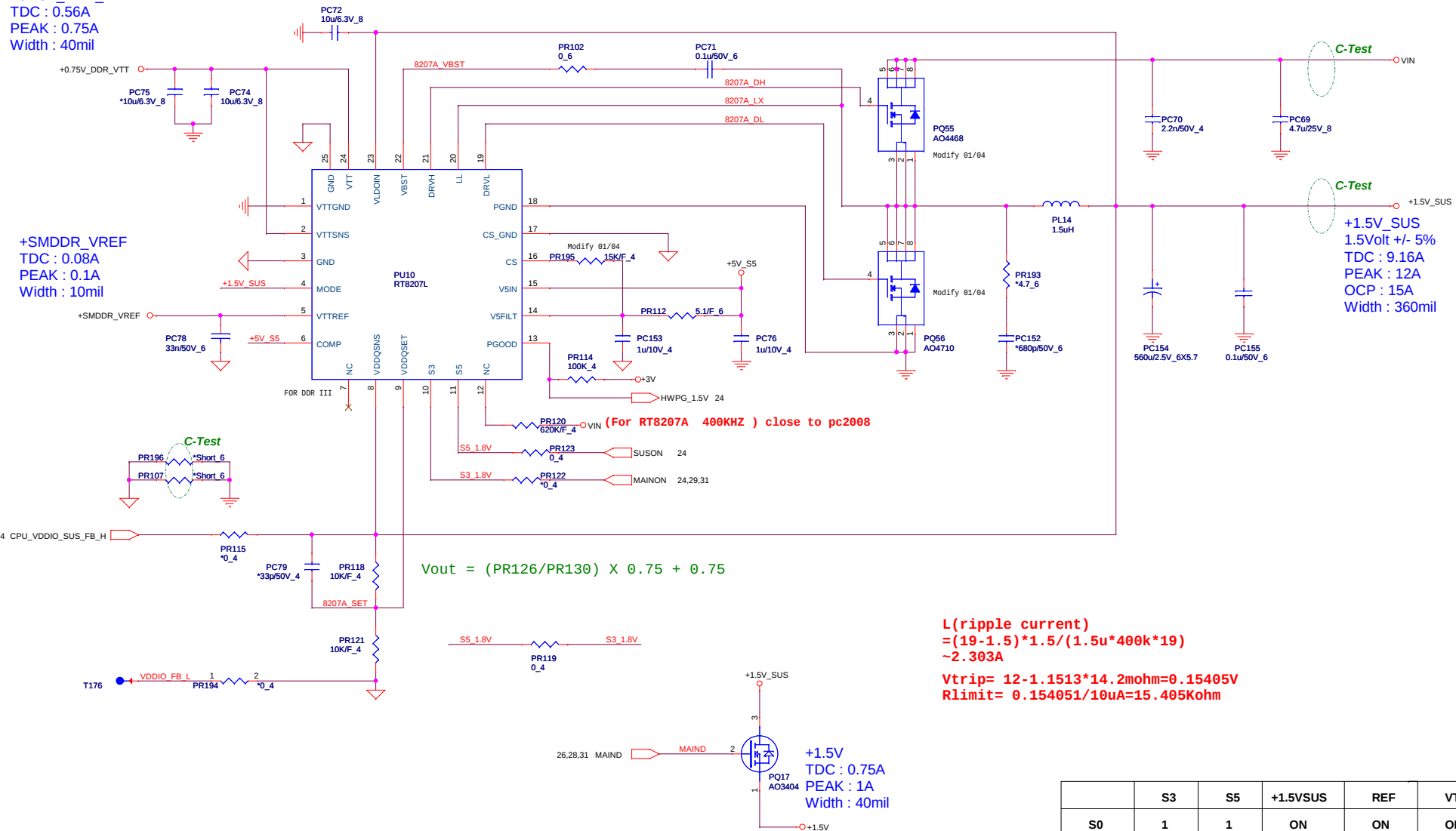
Size	Document Number	Rev
	VCCP 1.1V(UP6111A)	1A
Date:	Monday, February 21, 2011	Sheet 28 of 32



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+0.75V_DDR_VTT
TDC : 0.56A
PEAK : 0.75A
Width : 40mil

+SMDDR_VREF
TDC : 0.08A
PEAK : 0.1A
Width : 10mil

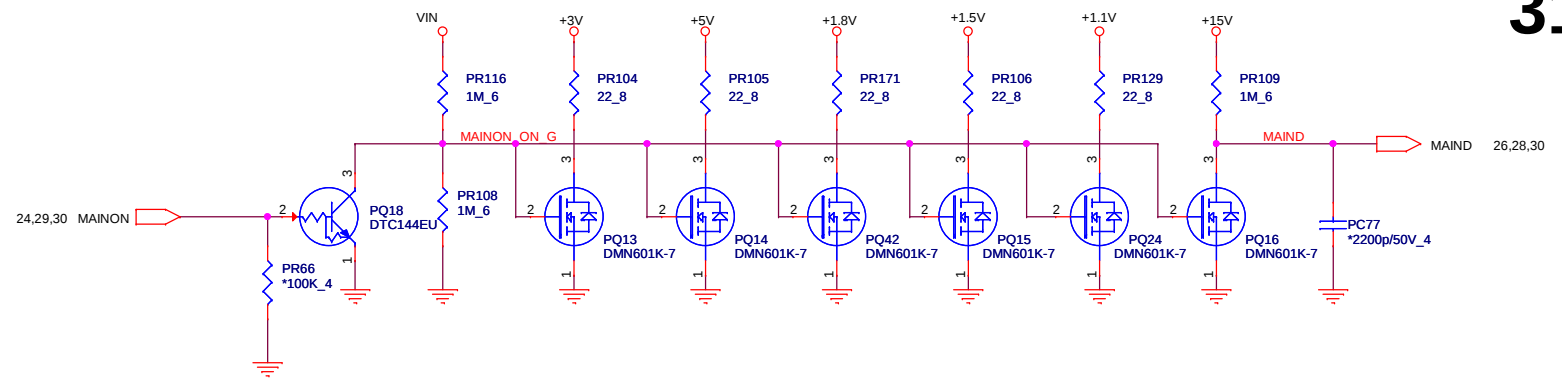


	S3	S5	+1.5VSUS	REF	VTT
S0	1	1	ON	ON	ON
S3	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF

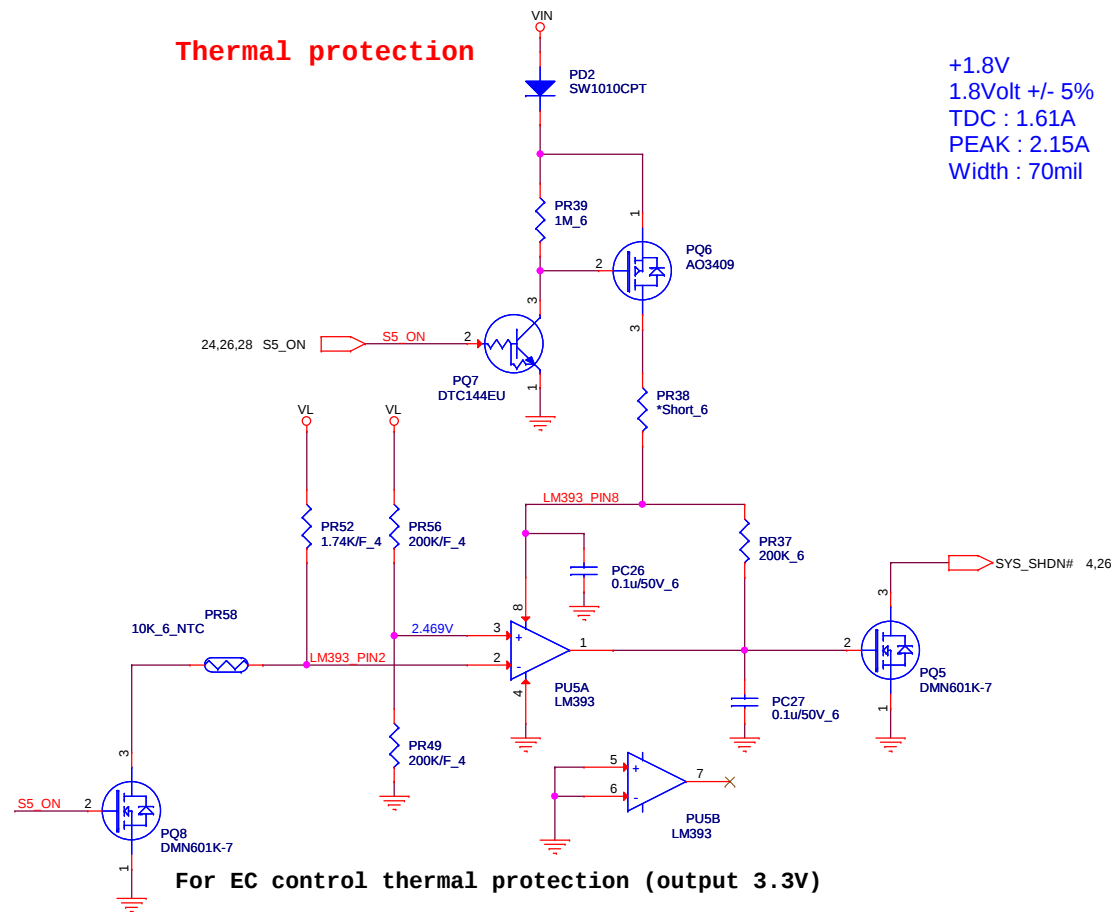


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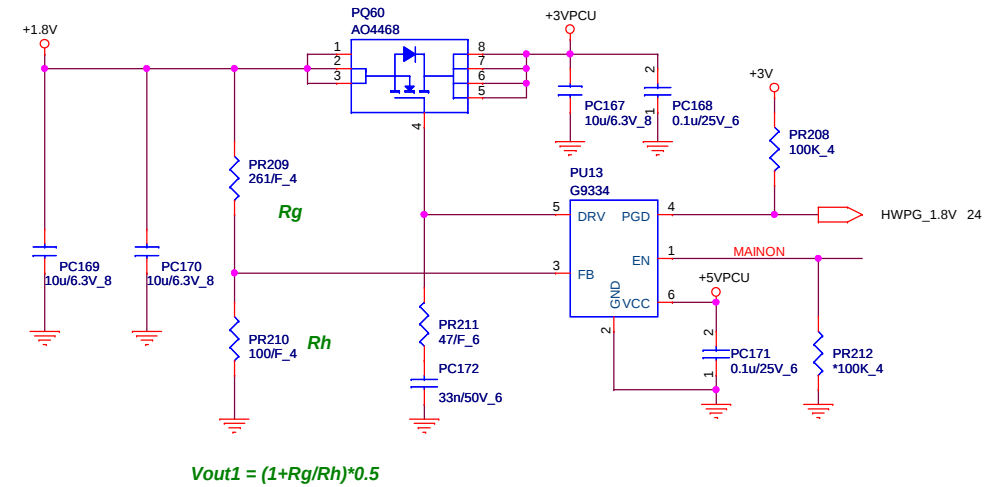
Size	Document Number	Rev
	DDR 1.5V(TPS51116)	1A
Date:	Monday, February 21, 2011	Sheet 30 of 32



Thermal protection



+1.8V
1.8V ± 5%
TDC : 1.61A
PEAK : 2.15A
Width : 70mil



PROJECT : ZQP
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Size	Document Number	Rev
	Discharge /Thermal protection	1A
Date:	Monday, February 21, 2011	Sheet 31 of 32

MODEL	REV	CHANGE LIST	Model ZQE/G M/B BOARD		
			Page	From	To
ZQP/Q M/B	A	First Release	1	1A	3A
			2	1A	3A
			3	1A	3A
	B	01.P14: Add HDMI function 02.P22: Add EC53,EC54 for EMI 03.P20: Stuff C673/C675/C671/C672 for EMI 04.P15: Stuff ESD protector at R31/R32 for EMI 05.P10: GPIO 58 define to HDMI strap pin 06.P08: Add C606,C614,C619 for strong clock 07.P20:change C673,C675,C671,C672 for EMI 08.P19:change L48,L47,L35,L34 to CX08T601000 for EMI 09.P24:No stuff SW1,stuff D1 10.P24:Add D5 on S5_ON for ESD 11.P22:LED2 change single lens(blue) 12.P08:Del C623 13.P24:Del SW1 14.P13:Del R26,R27 and add RP5 for EMI 15.P15:Add EC38,EC40,EC43,EC46 for EMI 16.P28:change PR79 to 0 ohm and stuff PR77 and PC51 for EMI 17.P29:change PR76 to 0 ohm and stuff PR164,PC126 for EMI 18.P27:stuff PR69,PC43 for EMI 19.P17:change C617,C612,C539,C552 footprint form 1206 to 0805 20.P13:Swap USB nets between L50 and PR5 21.P13:Add R33,R34 for ESD 22.P15:change C354 to CH122GK1I10 for EMI 23.P22:change EC30,EC32,EC34,EC36,EC37,EC39,EC42,EC45,EC48,EC53 and stuff it for EMI 24.P26:Remove JP20,JP21,JP22,JP23 and change to short pad PR235,PR237 25.P27:Remove JP10,JP9,JP6,JP8 and change to short pad PR55,PR48,PR43,PR46,PR47,PR54,PR63,PR142,PR140 26.P28:Remove JP24,JP25 27.P29:Remove JP16,JP17 and change to short pad PR70,PR72 28.P30:Remove JP18,JP19 and change to short pad PR196,PR107 29.P22:No stuff HOLE9	4	1A	3A
			5	1A	3A
			6	1A	3A
			7	1A	3A
			8	1A	3A
			9	1A	3A
			10	1A	3A
			11	1A	3A
			12	1A	3A
			13	1A	3A
			14	1A	3A
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			38	1A	3A
			39	1A	3A
			40	1A	3A
			41	1A	3A
Quanta Computer Inc. ZQP/Q		PROJECT: ZQP/Q	PCBA NO.	REV: 3A	DOC. NO :
APPROVED BY : Andy Lin		CHECK BY : Jia Huang	DRAWING BY : Andy Chen		DATE :10/18/2010
		SHEET 1			